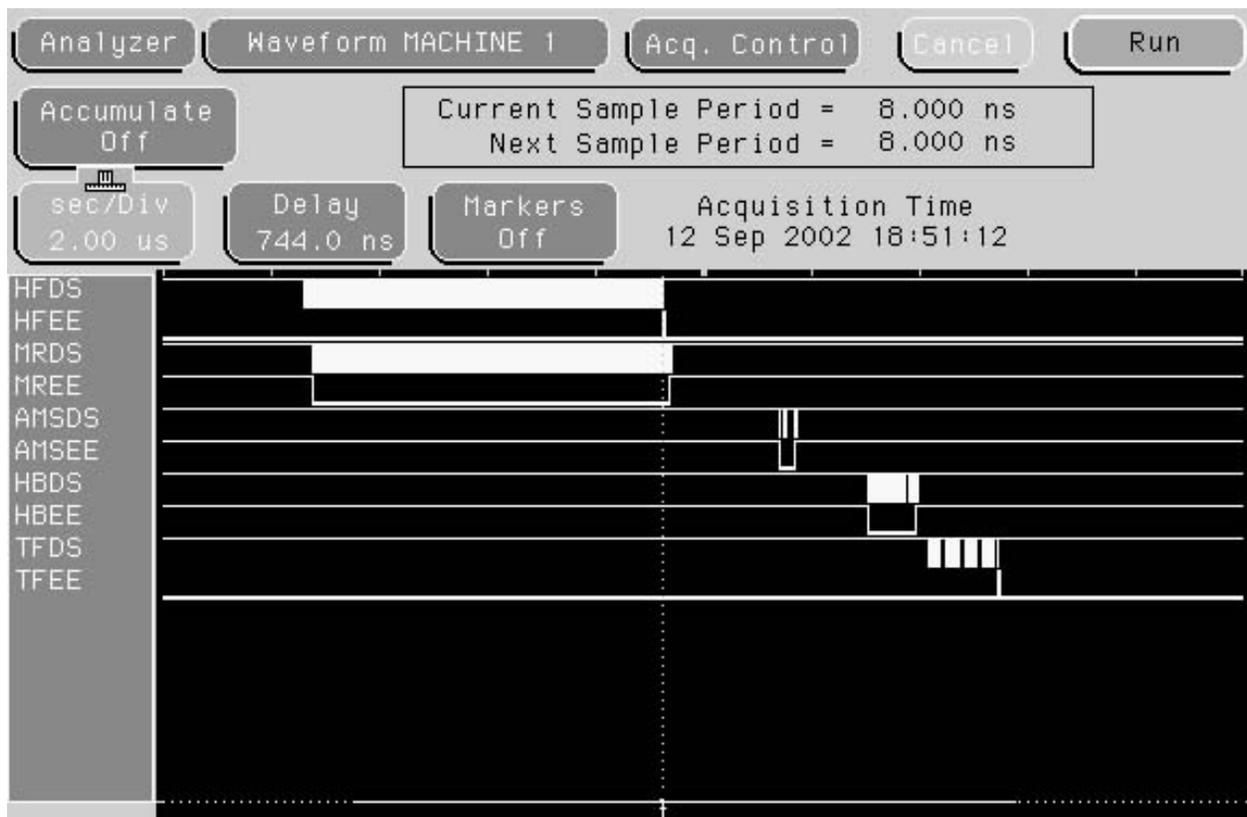


SVT timing studies

Status at September 16 (when I left) :

- The TTL DS & EE bits were connected to a couple of test points mounted on the front panel of SVT boards in the test-stand:
 1. HB
 2. MRG
 3. AMS
 4. TF
 5. HF (plus a signal from G-Link)
 6. L1A signal already from the SC
- Thanks to Bill's help we were able to send a simulated event to the teststand boards and to capture the event through an HP logic analyzer

Snapshot of the captured event: (from SVT logbook)



- I'm coming next Monday to go on this item
- First I want to replicate the work done at the teststand + study of the “statistics mode” of the LA

- Then we have to decide how to proceed:
 1. Do we move the modified boards to a real SVT sector ?
 2. Can we use the 2nd SVT output from HF to connect to a spare SVT chain, starting from a Merger ?
 3. Do we continue to work with the LA or try to use a GB as LA, reading back the timing values from VME ?
 4. Other ideas ?

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