



# L2 Trigger Commissioning

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Trigger Commissioning Workshop



## L2 Decision Crate

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- **Main Goals for Commissioning Run**
  - Used as final integration test for complete system
    - Verify correct data transfer into L2 processors
      - Will need to develop monitoring/diagnostic code
    - Study transfer time for each subsystem
    - L2 processor will send auto L2A or simply prescale selected L1A
  - Study performance capability of system
    - Run trigger algorithms
      - Initially run in tagging mode
      - Make a run where L2 does more than prescale
    - Run with high L1A rate - modify L1 thresholds as necessary
    - Understand sources of deadtime caused by L2



# L2 Processor Status

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- **Hardware**

- 1 Pre-production board at B0
  - Used for integration tests
- Tests with TS in calibration mode
  - L2 processor prescaled L1A by 1000, (TS interval 0 set to 5.)
  - Took 6.3us per event. Includes all L2 processor “overhead” needed for real running
    - Checks for L1A, configures buffer for receiving data, sends STARTLOAD, checks that data has been sent, handshakes L2 decision with TS
    - 6.3 us time can be reduced by 1-2 us with changes to fpga design
  - Ran over 600 million “events” (no readout of events)
- Expect 4 more production boards from ADCO “any day now”
- Sept 1. Will have single board in cosmic ray running
  - Likely to have 4 working boards at B0 by Sept. 15

8/17/00 Nov 1. Have 5 working boards



# L2 Processor

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- **Status - software**
  - Have “infrastructure” code for interfacing with trigger control system
  - Have code written for all triggers in CDF4718 (Work by Stephen Steffes)
    - Preliminary timing studies of triggers show processing times 0.5- 5 us per trigger
    - Have written a few Cosmic Calorimeter triggers
  - Run Control code
    - Current code is loaded in a standalone way (or automatically at powerup/reset)
      - Stays in loop checking for begin run. Responds to H-R-R
      - Loading a new executable is done by hand
    - Simple readout code written by Frank Chlebana (needs modification to read variable bank size)
    - Need to write code for executable creation based on Trigger DB
      - Work won't be done until early October



# L2 Processor

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- **Status - software**
  - Trigsim++Trigmon
    - Used to ensure correct data being sent to L2
      - Method for checking performance of interface boards
      - Initially will simply check data produced by TL2D with expected data based on other banks.
    - Have updated bank format in CDF4152 - Simona updated TL2D\_StorableBank.hh
    - Need to write code to fill bank
    - Need to write code for Trigmon
    - Eventually include L2 processor algorithm code in Trigsim



# Interface boards -Status

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- **L1 Trigger - Greg Feild**
  - **Hardware status and Testing**
    - Single prototype at B0
    - Successful single transfer integration tests done with old Fred
    - Need to verify operation with new Fred (problem with new cables)
  - **Software**
    - Will write simple code to compare TL2D and TL1D banks to verify data transfer
    - Trigsim modules need to be written for both Fred and L2 processor
  - **Expected working date**
    - Sept 1 realistic date for use of board in Cosmic Ray run
      - Will require dedicated debugging effort with Greg
    - 2 bare boards waiting to be stuffed for spares



# Interface boards -Status

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- **Track/SVT - Jane Nachtman**
  - **Hardware status and Testing**
    - Two prototypes being debugged using emulator
    - Tests of receiving data from SVT and XTRP were successful
    - Single word transfers to Alpha tested - still need to test multiple word
    - Have tested DAQ readout (with fixed block size) - variable size soon
  - **Software**
    - Standalone VME code for integration tests
    - Work started on a Trigmon package
  - **Expected working date**
    - Boards will not be fully tested by Sept. 1
      - Need to concentrate on integration tests in early Sept.
    - Should have fully working prototypes by Nov 1, send out production order



# Interface boards -Status

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- **Cluster List - John Carlson**
  - **Hardware status and Testing**
    - Single production board in integration tests at Michigan
    - Successful transfer of multiple events from DCAS->Clist->Alpha
    - Need to verify functionality of all 6 Hotlink inputs and using 6 DCAS
  - **Software**
    - Have standalone VME code to do data transfer integration test
  - **Expected working date**
    - Fully working board possible by Sept. 1
      - Will require full time effort over next 2 weeks
    - Arrival at B0 in mid-Sept., similar schedule to DCAS.
    - Should have fully working board by Nov 1
    - Will stuff 2 more bare boards at Michigan for spares



# Interface boards -Status

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- **Isolist - Steve Kuhlmann**
  - **Hardware status and Testing**
    - 2 working boards (1 needed)
    - Successful transfer of data from Isopick->Isolist->Alpha (at B0)
    - Problem losing seeds at high rate (1 us between seeds) fine at low rate
  - **Software**
    - Have standalone VME code to do data transfer integration test
  - **Expected working date**
    - Above problem probably a straightforward fix
    - Complete Isolation system by Sept. 15



# Interface boards -Status

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- **Reces - Karen Byrum**
  - **Hardware status and Testing**
    - 1 board tested at B0. Data transferred SMXR->Reces->Emulator
    - Alpha can write to board but not read from it
      - Problem with Alpha fpga design
    - 2 boards built but not tested. 3 more boards to be built
  - **Software**
    - Have standalone VME code to do data transfer integration test
    - Need to initialize SMXR with trigger thresholds
  - **Expected working date**
    - Sept. 1: 1 Board working at B0 handles 12 wedges (only 2 instrumented)
    - Nov 1: Will have 3 boards working at B0
      - Likely all 4 needed boards operational by Nov.



# Remaining Integration Tests

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- Full crate test at B0
  - 1 interface board to 4 Alphas
  - Fill crate with full set of boards to load backplane
    - Use standalone code to do single board transfer tests
    - Check that all 4 Alphas receive data
    - Test won't happen until mid-Sept. at earliest
- L1A signal
  - Check for proper operation of interface boards after L1A
    - Need to develop code and procedure for this test
    - Similar to actual running conditions
- Error conditions
  - Proper recovery after error condition
  - Method to quickly identify board causing failure



# Summary- Thoughts

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## – Integration tests

- Much integration testing done with Alpha + single board
- Many boards still need individual testing/fixes
- Full system integration will likely reveal new problems
- Need to be able to easily remove/add L2 crate to cosmic/commissioning runs
- Will use 2nd L2 crate to do integration tests in parallel with run

## – (No Surprises) Schedule

- By Sept. 1 - L2 crate in cosmic run with 1 Alpha, L1 interface board, TL2D bank readout
- By Sept. 22 - Cluster list and Iso-list boards installed along with full L2 Cal system
  - Finished Alpha-Reces integration tests
  - First round of full crate integration tests done
- By Sept. 31 - Working Track/SVT boards in L2 crate, readout by DAQ