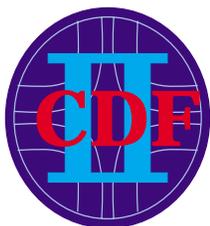




CDF Run IIb Trigger & Data Acquisition Upgrades

Kevin Pitts
University of Illinois
for the CDF Collaboration
August 13, 2002



Run IIb Trigger/DAQ Upgrades

Talk Outline:

- **Motivation**
 - *Run IIb physics goals*
 - *Trigger strategies*
- **Specific projects** ←
- *Specific issues*
- *Design*
- **Cost**
- **Schedule**
- **Conclusion**

The upgrades:

- **TDC replacement**
 - *Central tracker readout*
- **XFT upgrade**
 - *Level 1 track trigger*
- **SVT**
 - *silicon vertex trigger*
- **Level 2 trigger**
 - *Level 2 decision crate*
- **Event builder/Level 3 processor**
 - *Data acquisition*



Motivation

- The upgrades presented here are driven exclusively by our Run IIb trigger and data acquisition needs to carry out our high- p_T physics program
- Our current level of understanding is based upon
 - Run IIa data: $L \leq 2 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$, **~1 interaction per crossing**
 - Run I data: $L \sim 2 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$, **~2 interactions per crossing**
- We are extrapolating to Run IIb
 - $L = 2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ w/396ns bunch spacing (**~5 int/beamX**)
 - $L = 5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ w/132ns bunch spacing (**~5 int/beamX**)
 - **Due to significant uncertainties in extrapolation, and a desire to be prepared for success, we have evaluated our system for:**
 $L = 4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ w/396ns bunch spacing (**~10 int/beamX**)



Trigger Strategy

- Focus on Higgs & high p_T searches
 - Know that triggers needed for these modes will allow for many beyond Standard Model searches
- General requirements:
 - High p_T electrons and muons
 - Associated WH/ZH modes, also $t \rightarrow Wb$
 - Missing E_T triggers
 - ZH with $Z \rightarrow \nu\bar{\nu}$, modes with taus
 - b -jet triggers
 - $H \rightarrow b\bar{b}$, b -jets tagged by displaced tracks
 - Calibration triggers
 - $Z \rightarrow b\bar{b}$, $J/\psi \rightarrow \mu^+\mu^-$, photons



Run IIb Trigger Table

trigger path	$\sigma_{L1}(\text{nb})$	$\sigma_{L2}(\text{nb})$	$\sigma_{L3}(\text{nb})$
High E_T electron	1,500	170	30
Plug electron + missing E_T	771	55	10
High P_T muon (CMUP)	1,773	200	8
High P_T muon (CMX)	1,773	200	8
2 high p_T b -jets	10,840	200	10
missing E_T + 2jets	163	126	13
jets	6,500	42	12
missing E_T	overlap	163	3
Photons	overlap	50	15
$J/\psi \rightarrow \mu^+ \mu^-$	850	38	10
High P_T jets	19,000	60	17
hadronic top	overlap	50	5
di- τ	5,000	50	4
missing $E_T + \tau$	overlap	50	4
High E_T photons	13,500	110	21
dileptons, trileptons	1,000	190	45
total	59,200	1904	215



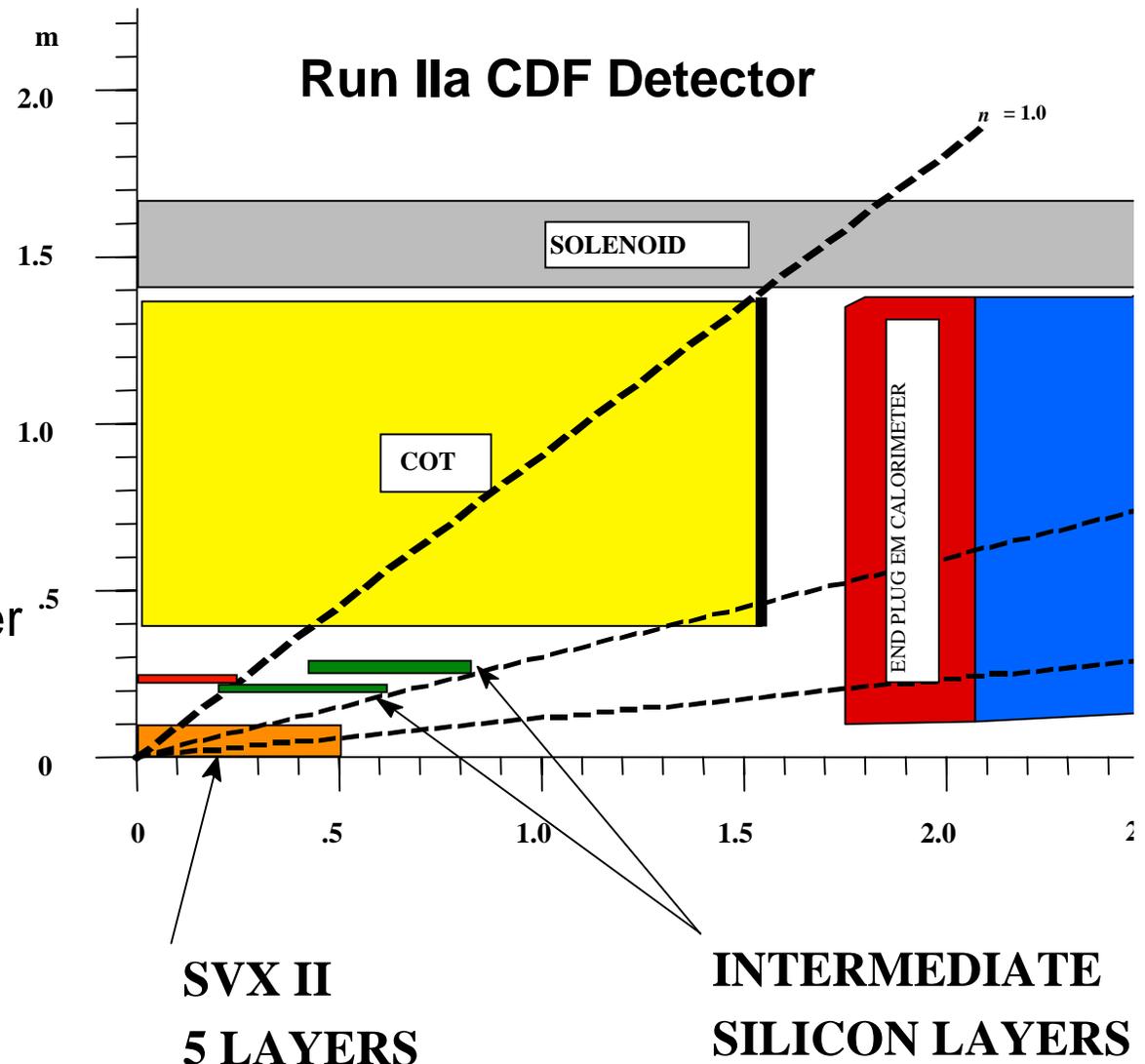
Summary of Run IIb specifications

- **Level 1 Accept rate: $>25\text{kHz}$ (spec 50kHz)**
 - **deadtimeless**
- **Level 2 Accept rate: $750\text{ Hz} \rightarrow \text{bursts to } 1.1\text{kHz}$**
 - **L2 processing deadtime $< 5\%$**
 - **readout deadtime (on L2A) $< 5\%$**
- **Level 3 Accept rate: 85Hz**
 - **Event builder rate: 400MB/s**
 - **Output data rate: 40MB/s**
- **Reminder: trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)**



The CDF Detector

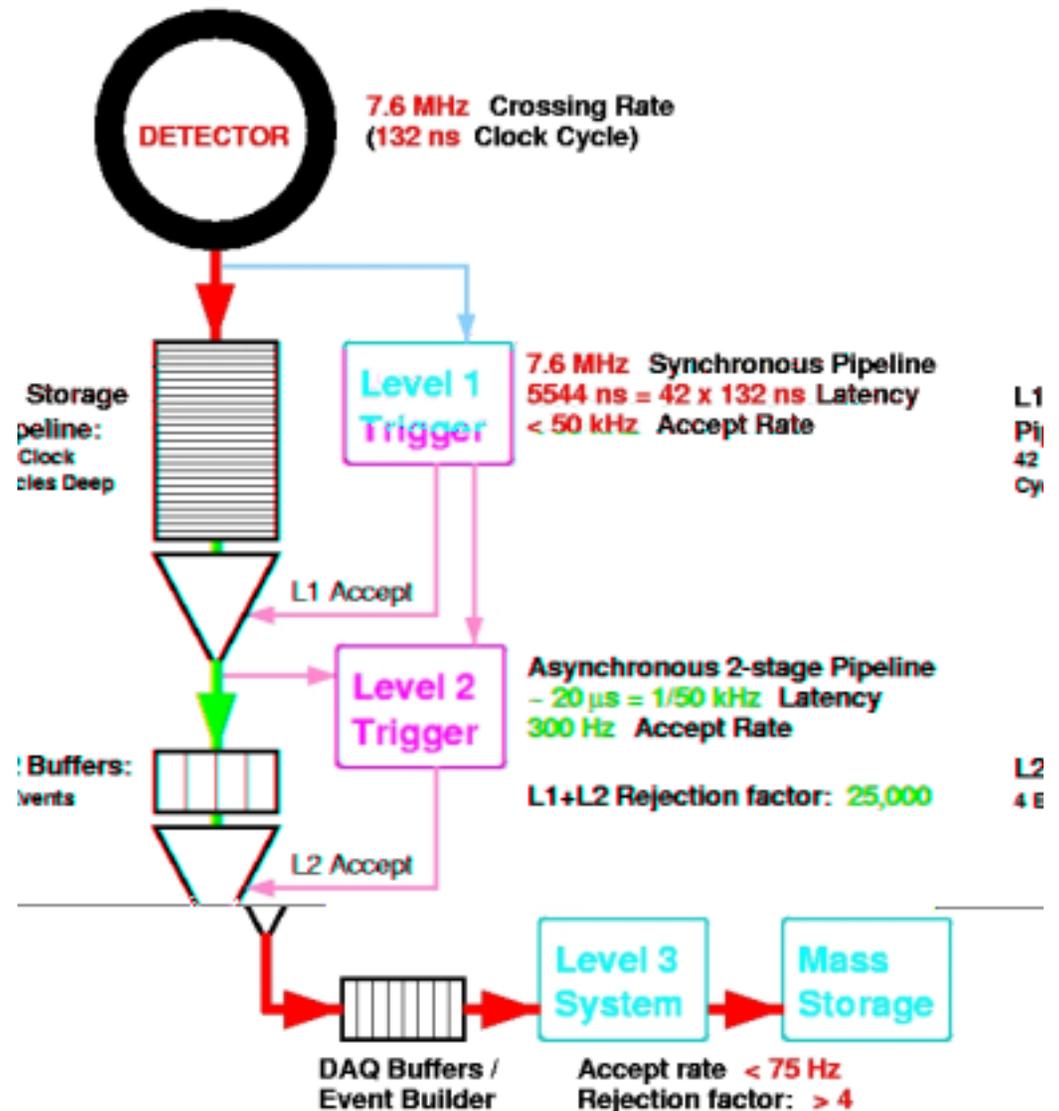
- Important detector element for this talk is the Central Outer Tracker (COT)
 - drift chamber with 30k sense wires
 - solenoid field is 1.4T
 - track needs $p_T \sim 75$ MeV to get to COT inner layer
 - tracks with $|\eta| < 1$ pass through all COT layers
 - inner layers see tracks with $|\eta| < 2$





CDF Data Acquisition System

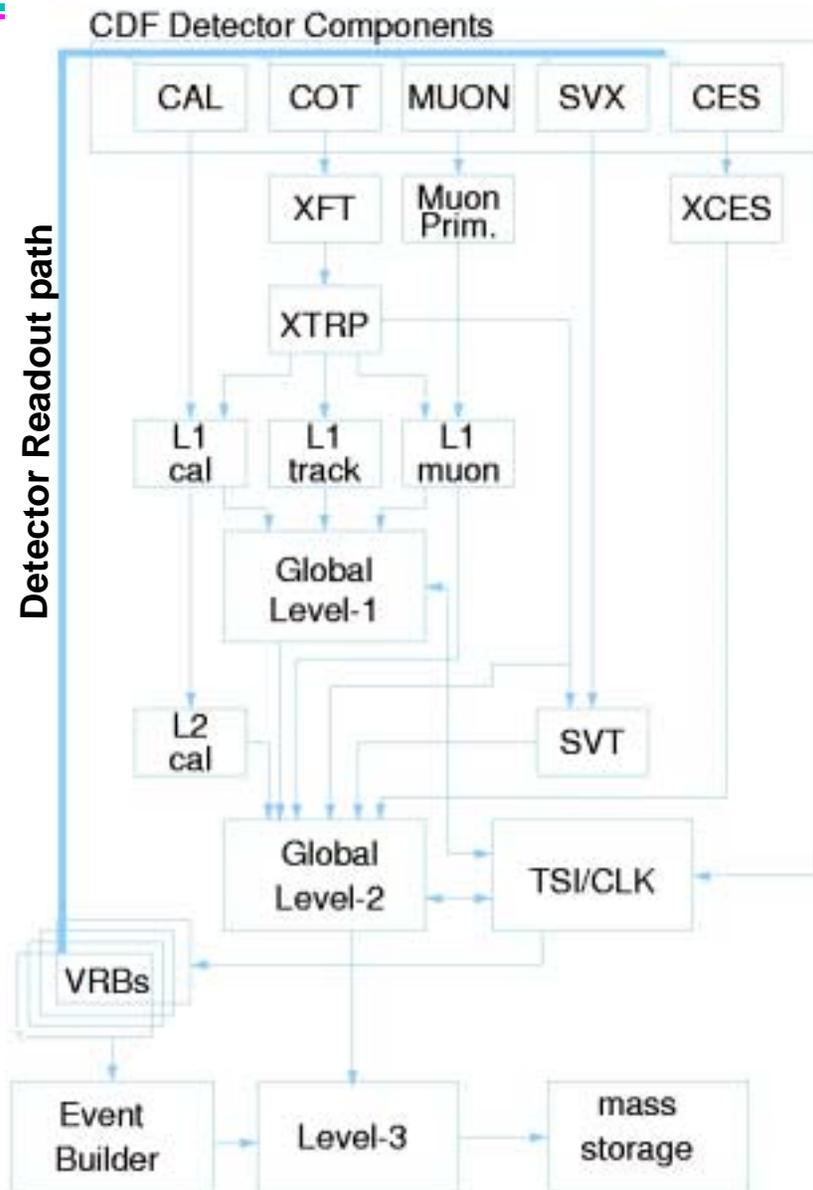
- Level 1 trigger
 - pipelined and “deadtimeless”
 - fully synchronous
 - designed for 132ns operation
 - on L1A, write data to 1 of 4 L2 buffers
- Level 2 trigger
 - asynchronous
 - L1 + supplemental info
- Level 3 trigger
 - full detector readout
 - PC farm runs reconstruction
 - output to mass storage





CDF Run II Trigger System

- Level 1 trigger
 - tracking
 - calorimeter: jets & electrons
 - muons
- Level 2 trigger
 - L1 information (tracks, e, μ)
 - calorimeter shower max
 - silicon information
 - algorithms run in L2 processor
- Level 3 trigger
 - full detector readout
 - “offline” processing

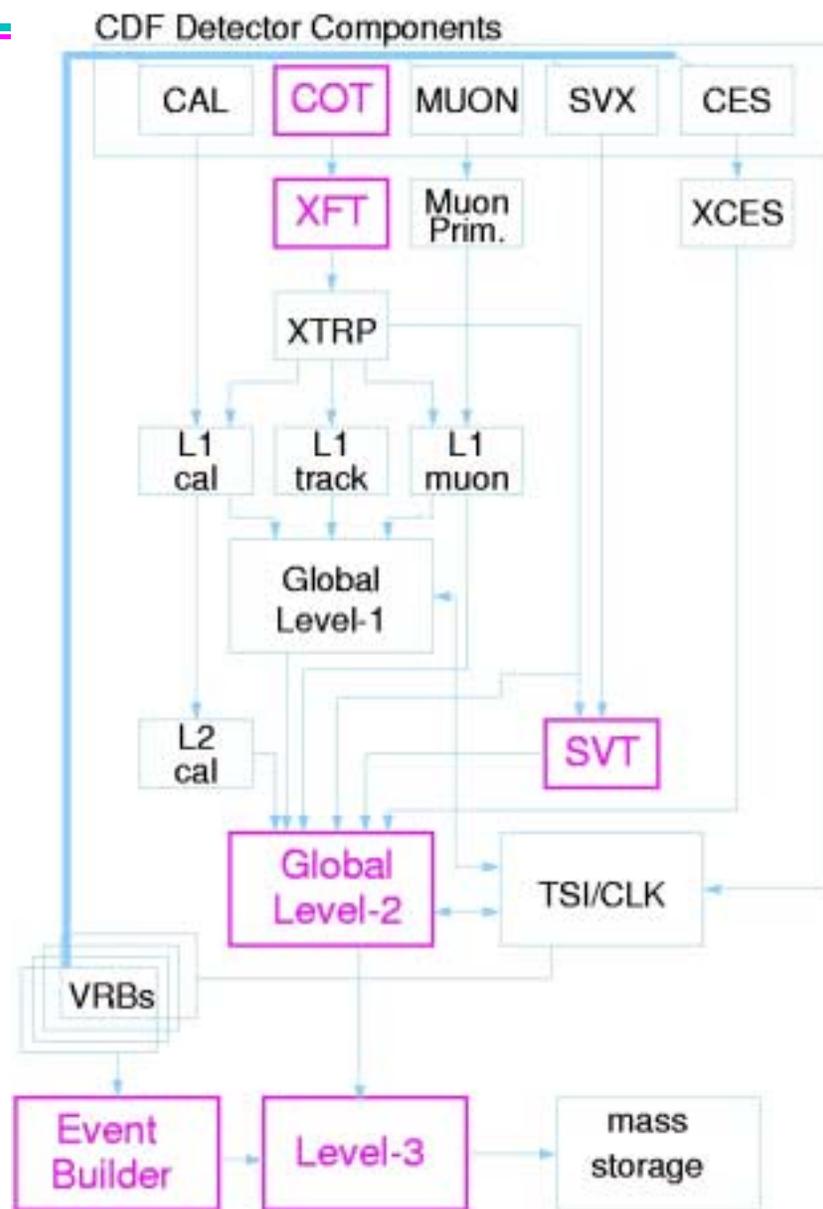




Trigger/DAQ Upgrades for Run IIb

General considerations:

- upgrades “targeted” to specific needs
 - e.g. COT TDCs replaced, but remaining COT readout (ASDQ, repeaters) unmodified
- retain existing infrastructure
 - cables, crates unchanged
 - I/O protocols, timings retained
 - upstream/downstream components unchanged
- upgrades plug compatible with existing components
 - take advantage of knowledge & experience
 - will aid in commissioning





COT TDC Upgrade

Central Outer Tracker (COT)

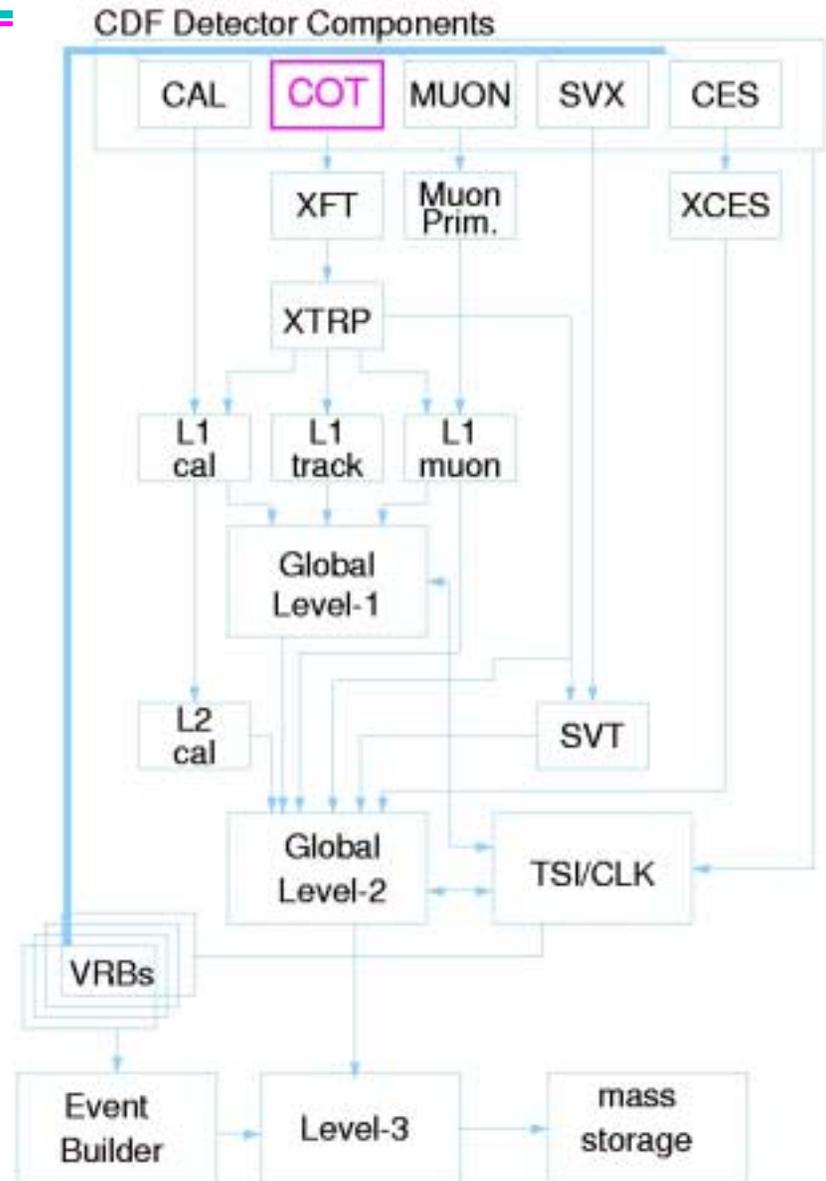
- central drift chamber

COT readout path:

chamber → ASDQ → microcoax →
repeater board → flat cable → TDC

ASDQ = amplifier shaper discriminator
with charge-encoding

TDC = time-to-digital conversion

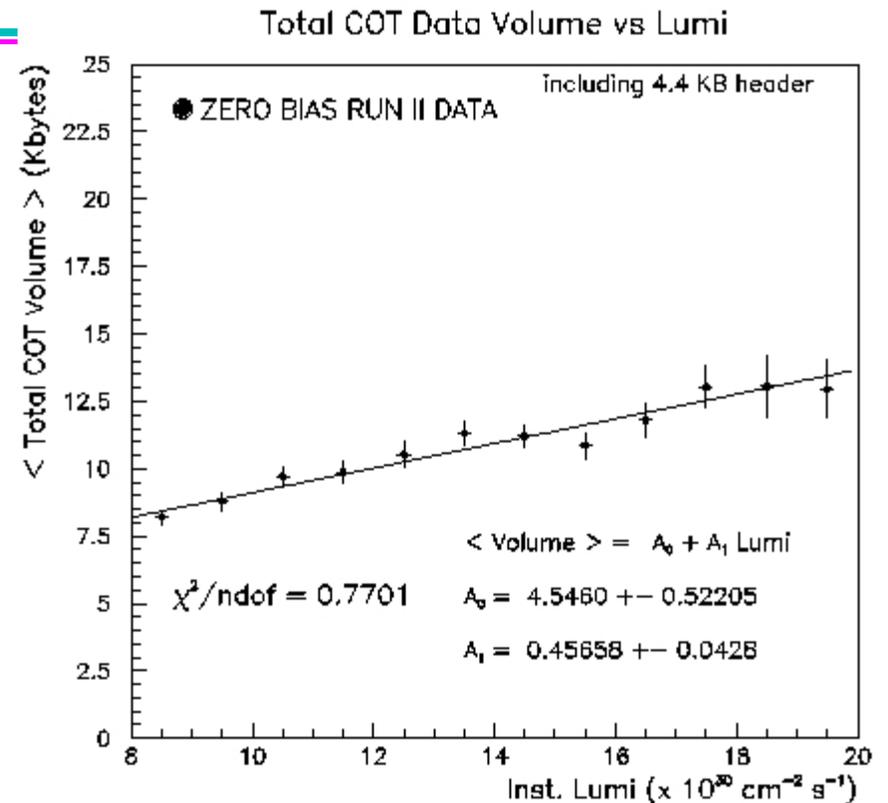




TDC Replacement

Limitations of current system:

- TDC on-board data processing
 - existing system performs hit processing after L2A
 - processing time (=deadtime) grows with # of hits
 - COT occupancy higher than expected
 - Run IIa processing time too large for Run IIb
- VME readout
 - 16 TDCs per crate read out serially by VME block transfer
 - current VME transfer rate 14MB/s with additional overhead per board
 - Run IIa, 300Hz...falls to ~150Hz (!) in Run IIb
- Data transfer
 - TRACER→TAXI→VRB link provides bandwidth limitation
 - maximum TAXI →VRB is <12MB/s...Run IIb requires 14MB/s





Run IIb TDC Performance

Specification: entire TDC readout must be completed within $600\mu\text{s}$ to handle 1.1kHz rate $\Rightarrow 14\text{MB/s}$.

- **TDC (on-board) processing time [time after L2A]**
 - Now: slowest TDC $>650\mu\text{s}/\text{event}$
 - Need $\sim 360\mu\text{s}$ to achieve 1kHz L2A rate
- **VME readout**
 - Currently: $\sim 500\mu\text{s}$ per crate
 - Run IIb: x10 more data $\Rightarrow >1\text{ms}$
- **Data transfer**
 - Run IIb: expect 14MB/s , TAXI link limited to $<12\text{MB/s}$
- **Internal CDF TDC Review committee convened in June**
Conclusion:
 - existing COT TDCs + VME readout system cannot maintain necessary L2A rate in Run IIb
 - TDC system must be replaced **OR** significant modifications to the DAQ & infrastructure must take place



New TDC Design

- Address on-board processing deadtime by moving hit processing into the L1→L2 transition
 - “hide” hit processing behind L2 trigger
- Address VME and Readout problems via bypassing the VME→TRACER→TAXI
 - Keep existing data path as a backup (commissioning)
 - Maintain other pieces of DAQ chain (VRB →EVB)
- Design exclusive to COT system, reduces constraints
 - Run IIa TDC will continue to work well for other systems (muons, hadron timing, CLC)



TDC Specifications

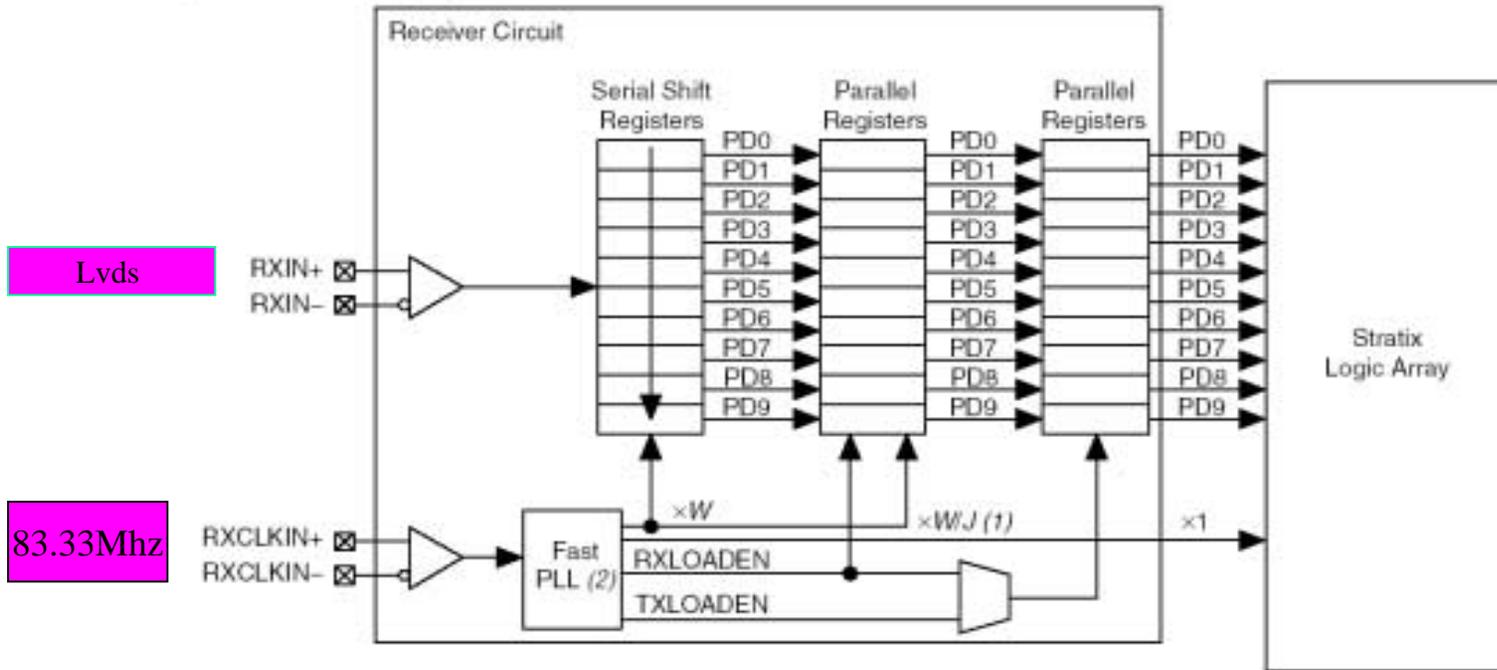
- Backward compatible with existing system
 - No change to COT front-end, cables or calibration
 - No change to track trigger (XFT) interface
 - Accept CDF specific signals from CDF_CLOCK/TRACER
- Must handle the following rates
 - 50kHz L1A, 1.1kHz L2A
 - Readout time below 500 μ s with 20kB/crate
- Allow for on-board data compression
- Perform hit finding for track trigger
- “TDC Specifications” document provides details



New TDC Design

- Done with Altera Stratix FPGA
 - commercially available
 - high bandwidth differential input ← matches COT
 - sufficient on-chip logic & memory to carry out all needed functions (with room to spare)
 - moderate price
- Time-to-digital conversion performed on chip input
 - 840MHz LVDS inputs
 - not sensitive to routing issues
 - remainder of FPGA functionality digital

Figure 3. Stratix High-Speed Interface Deserialized in $\times 10$ Mode



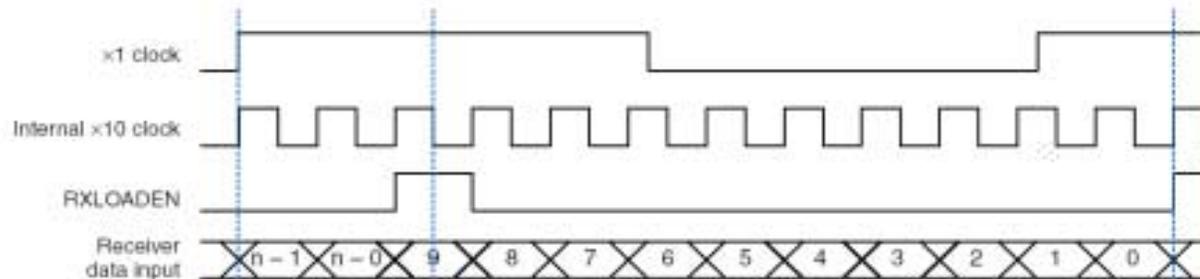
Notes to Figure 3:

- (1) $W = 1, 2, 4, 8, \text{ or } 10.$
 $J = 4, 8, \text{ or } 10.$

W does not have to equal J . When $J = 1$ or 2 , the deserializer is bypassed. When $J = 2$, the device uses DDRIO registers.

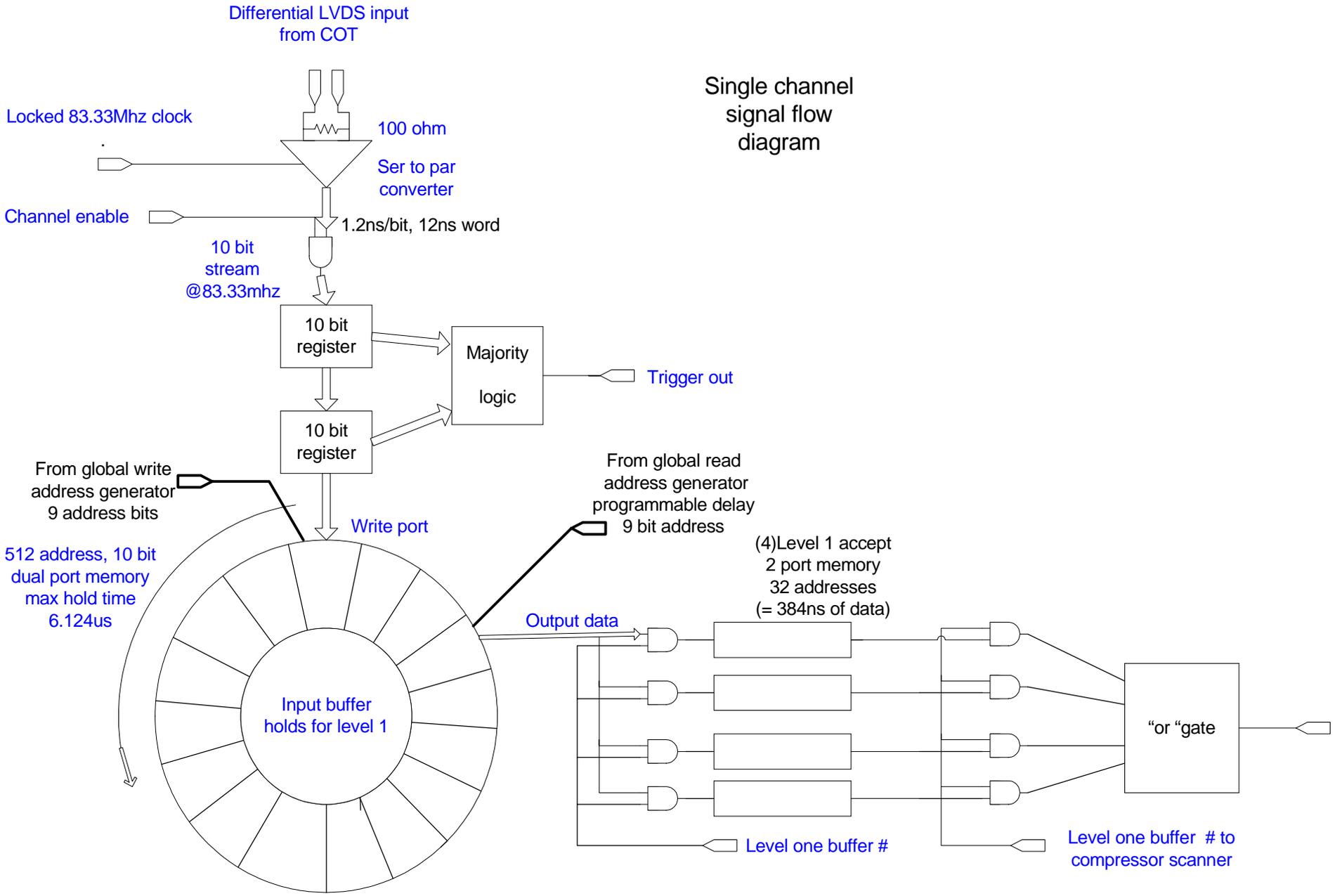
- (2) This figure does not show additional circuitry for clock or data manipulation.

Figure 4. Receiver Timing Diagram



ALTERA LVDS RECIEVER

Single channel signal flow diagram





TDC Readout

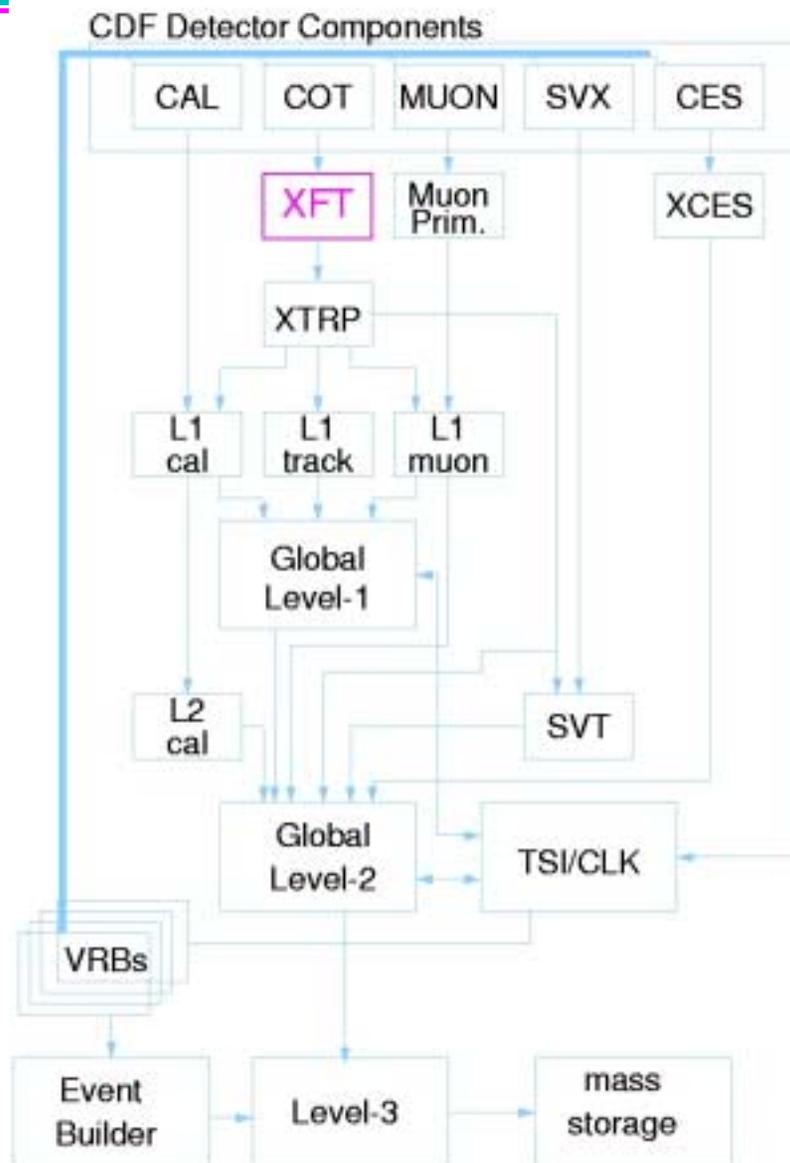
- TDC readout performed by G-link.
 - TDCs daisy-chained fiber optic to a data concentrator
 - concentrator ships data to VRB
 - VRB supports G-link for SVX readout
- TDC will support Run IIa VME readout for commissioning
 - will be able to install new TDCs into existing system for testing and timing resolution studies



eXtremely Fast Tracker Upgrade

XFT finds charged tracks
with $p_T > 1.5 \text{ GeV}/c$

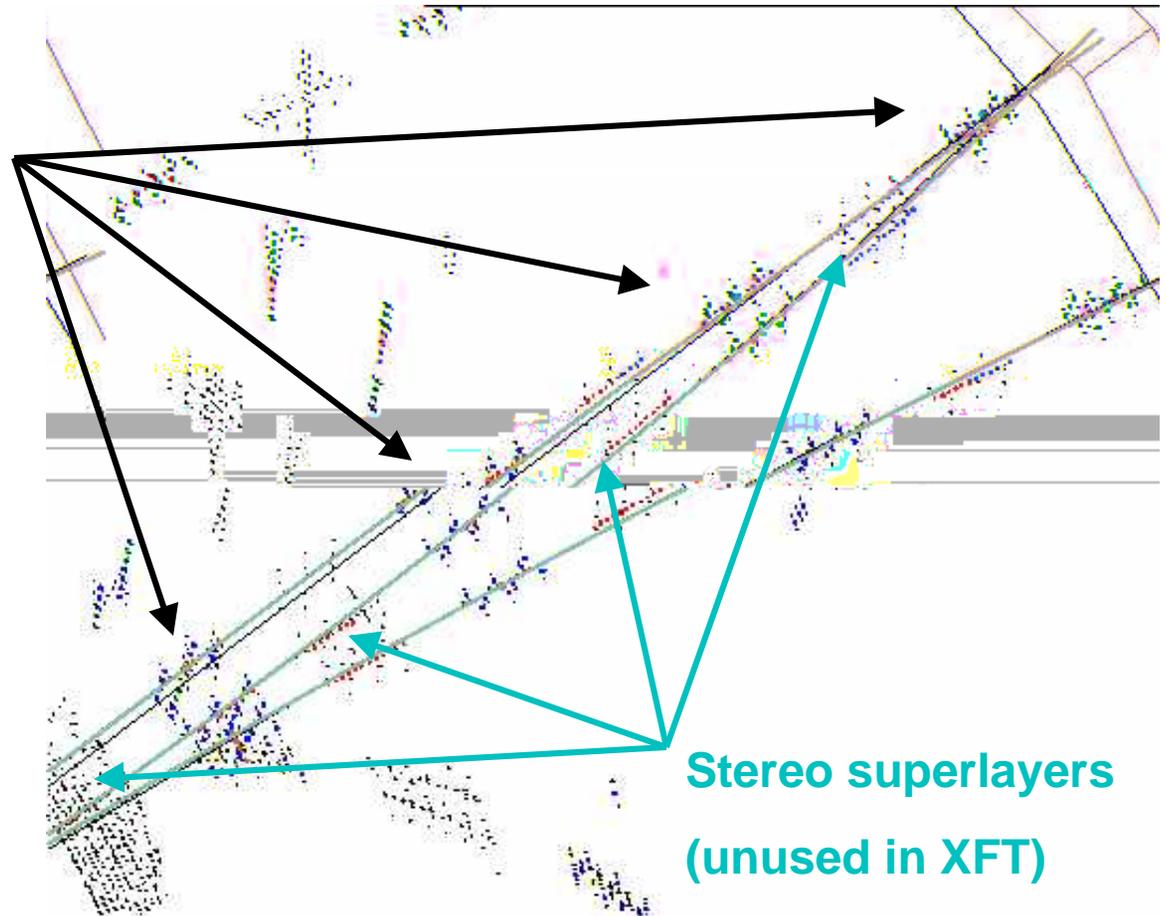
Part of the Level 1 Trigger system



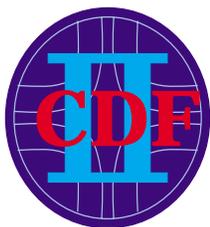


Run IIa Track Trigger System

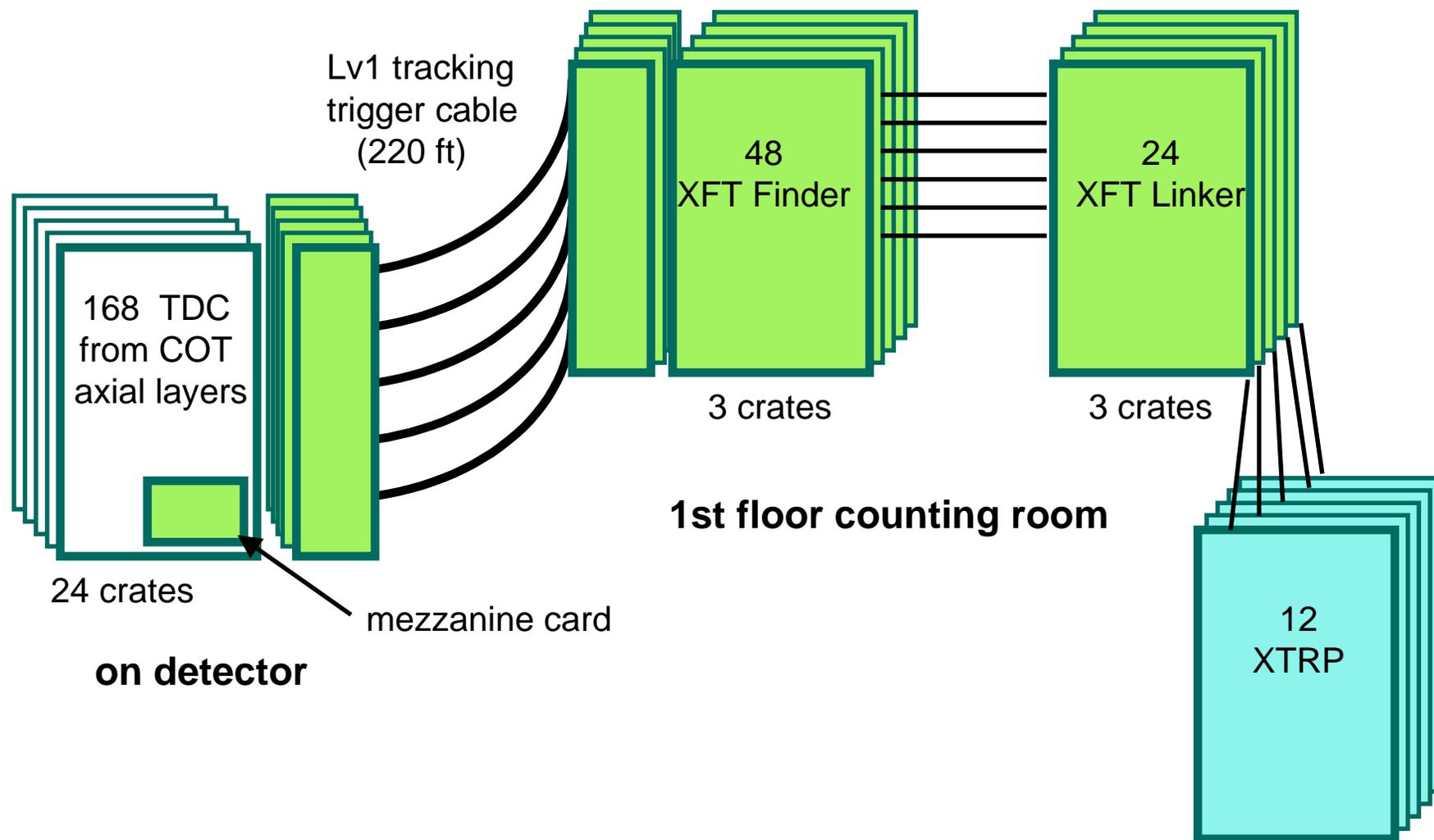
- XFT works by finding line segments in the four axial superlayers
 - “finder” boards
- Tracks are found by linking the segments into tracks
 - “linker” boards



✕ Interaction point



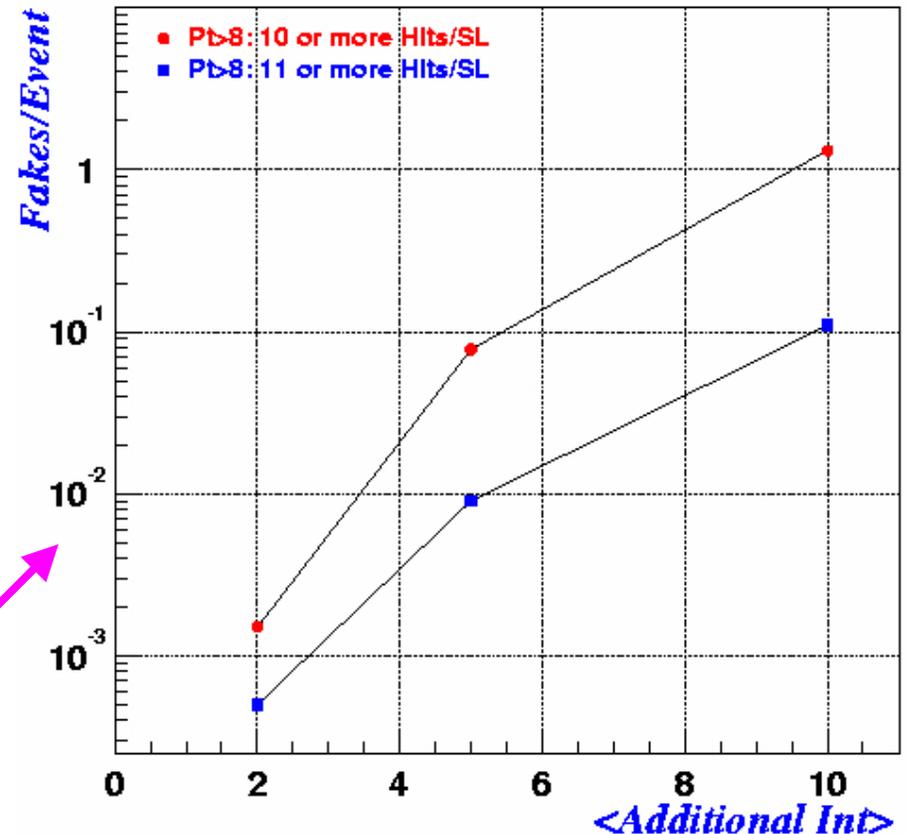
Run IIa Track Trigger System





XFT Upgrade

- Track-based triggers are responsible for >50% of the Run IIb physics program
 - e, μ , τ , b -tags
- COT occupancy at high luminosity causes significant L1 track trigger (XFT) degradation
 - Significant growth in fake track rate (primarily at high p_T)
 - Degradation in p_T and ϕ_0 resolution (next slide)



Inclusive electron events (data) superimposed on additional minimum bias events.

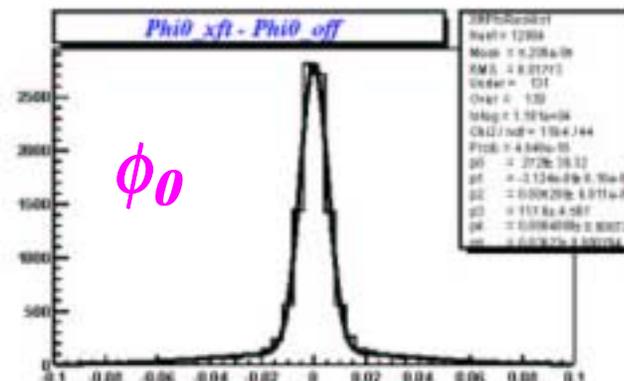
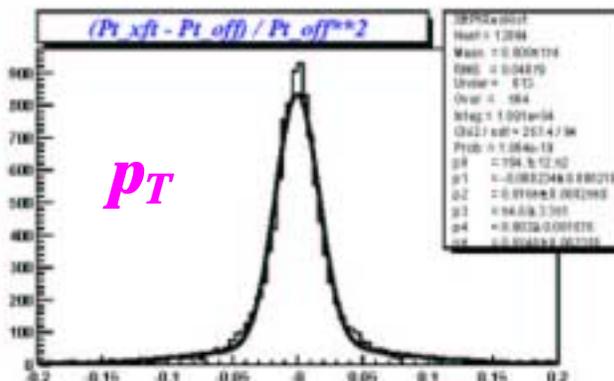


XFT p_T & ϕ_0 Resolution

Data: high p_T electrons

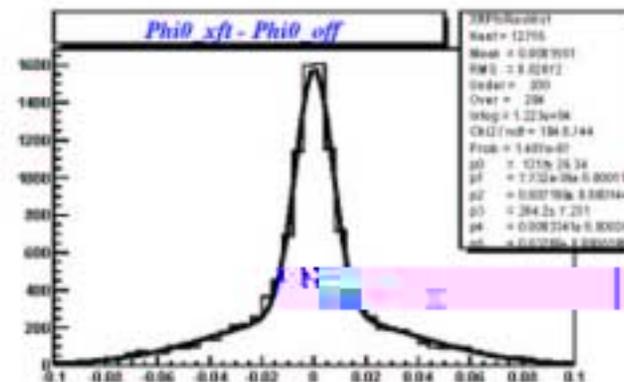
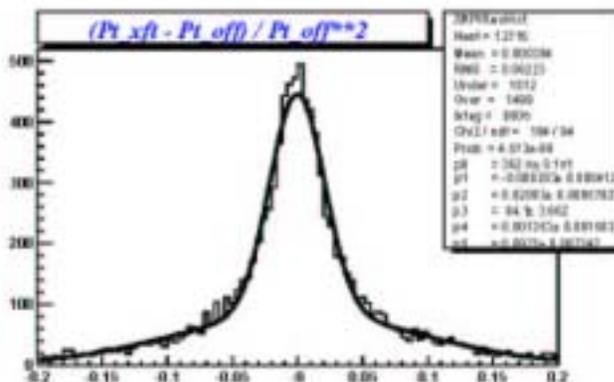
+0 minimum bias events

L = now



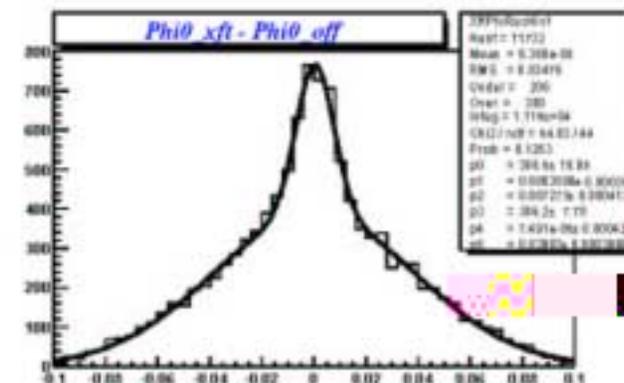
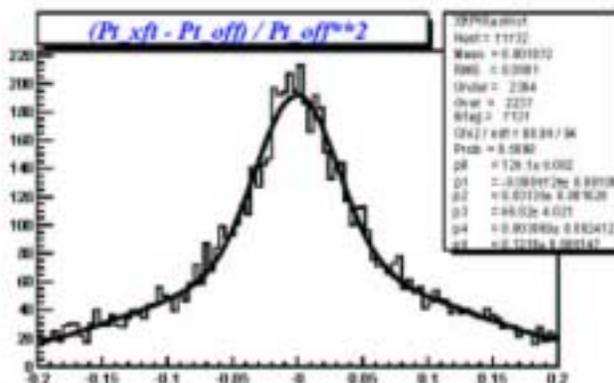
+5 minimum bias events

L = $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ @396ns



+10 minimum bias events

L = $4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ @396ns





XFT IIb Design

- **Reduce fakes and improve resolution with improved axial track finding & 3D information**
- Take advantage of existing design and infrastructure
 - Cables, I/O, data formats unchanged
- Difference between XFT & offline tracking is time binning. Segment angle match improves with finer time bins.

Upgrade:

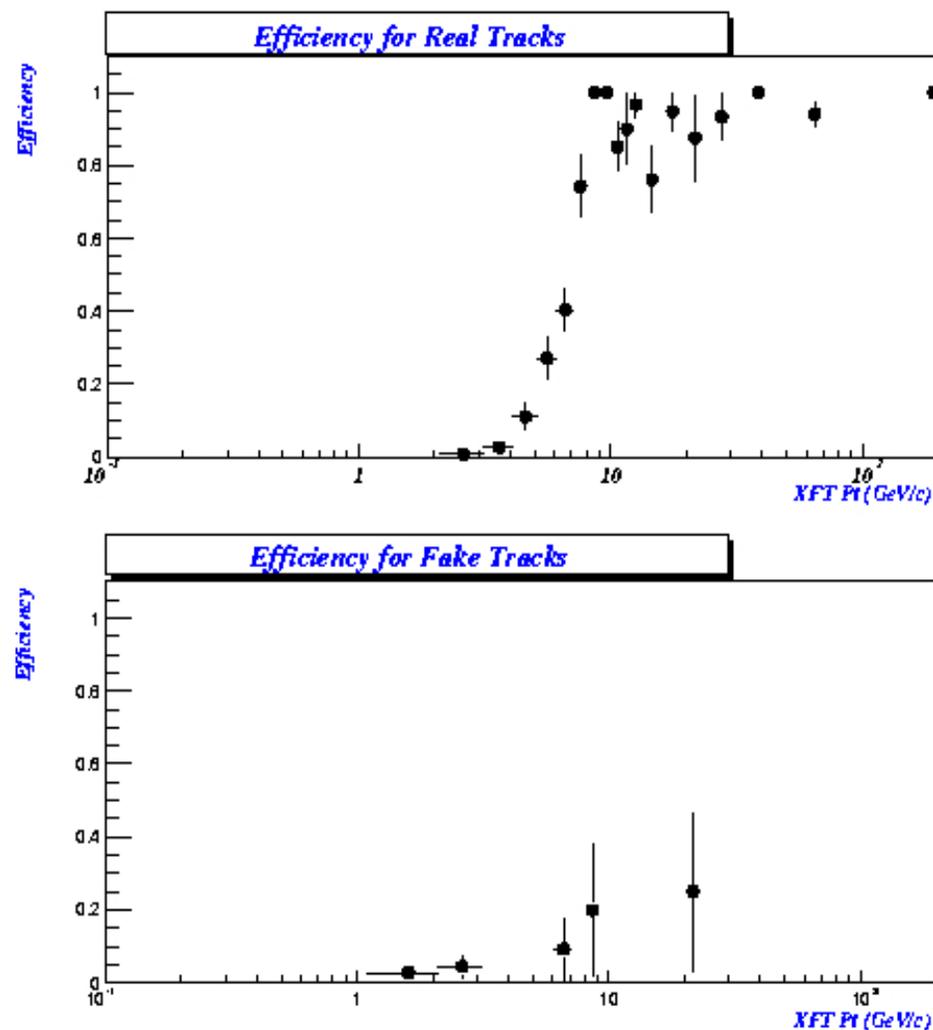
- ① Utilize 396ns baseline to pipe more information per beam-X from TDC→XFT.
 - Go from two time bins to six time bins in the trigger
- ② Supplement axial tracking with stereo measurement
 - Segment finding identical to axial XFT
 - Stereo information provides:
 - improved fake track rejection (important at high L)
 - new: electron & muon matching in η



XFT Upgrade Performance

- Additional timing information plus stereo provides high efficiency for tracks while keeping the fake rate low
- Plots shown are for 10 interactions/crossing
 - high efficiency
 - low fake rate
 - improved p_T and ϕ resolution

Histograms





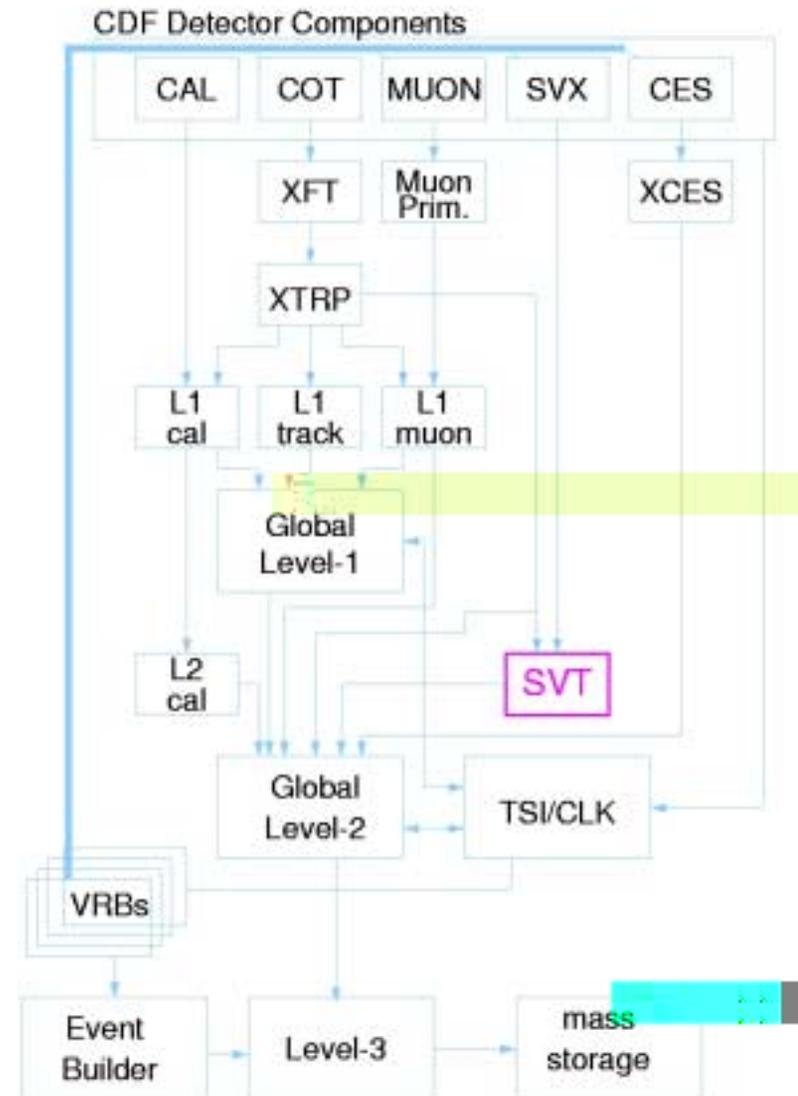
XFT Upgrade



SVT Upgrade

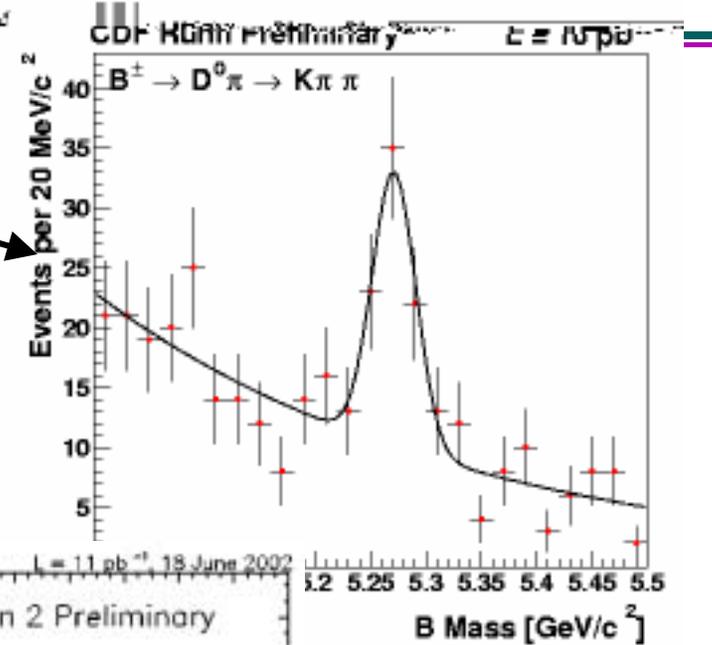
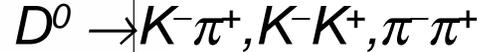
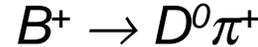
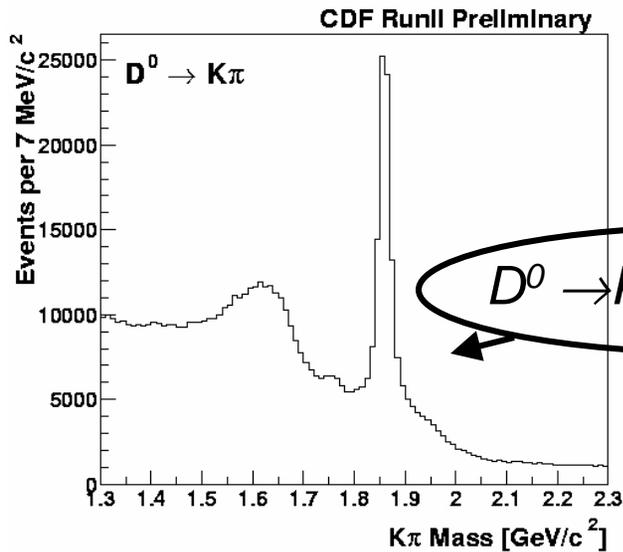
Silicon Vertex Tracker (SVT)

- brings axial silicon information into trigger
 - allows for cuts on impact parameter in trigger (!)
- In order to be fast, SVT must specifically handle
 - SVX readout
 - SVX geometry
 - Tevatron beam position

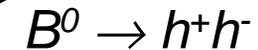
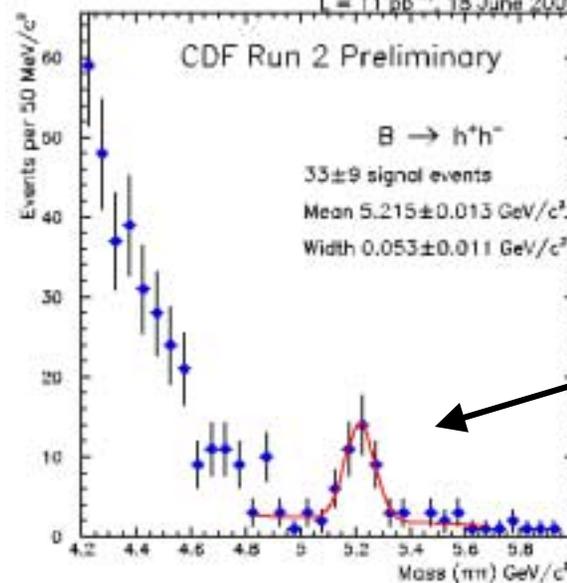




Run IIa SVT



- Silicon tracking information in the trigger
 - find displaced tracks
 - Run IIb, important for Higgs, SUSY, $Z \rightarrow b\bar{b}$

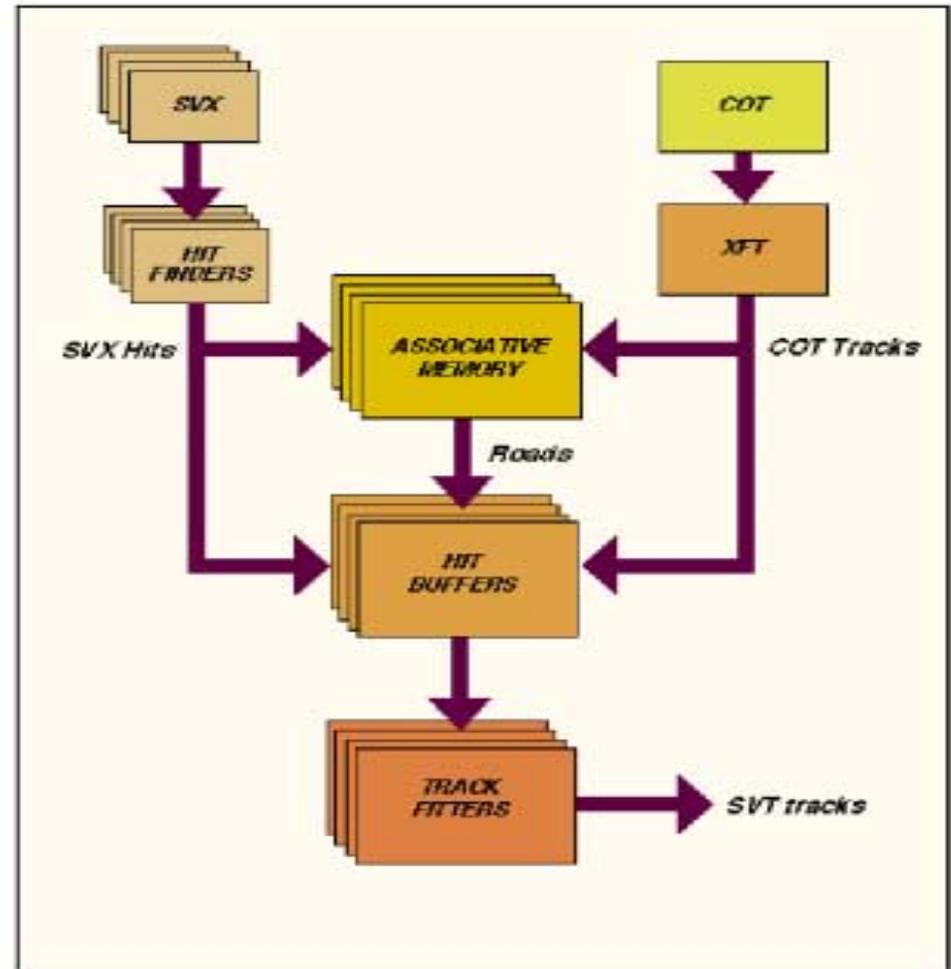




SVT Upgrade

- SVT is unchanged from the Run IIa system
- SVX IIb geometry different than SVX II geometry
- due to geometry change, SVT in Run IIb requires
 - 12 additional Merger boards
 - layout, functionality identical to existing boards
 - this item is production only
 - new Track Fitter boards
 - layout changes to handle geometry
 - function of board unchanged

SVT architecture

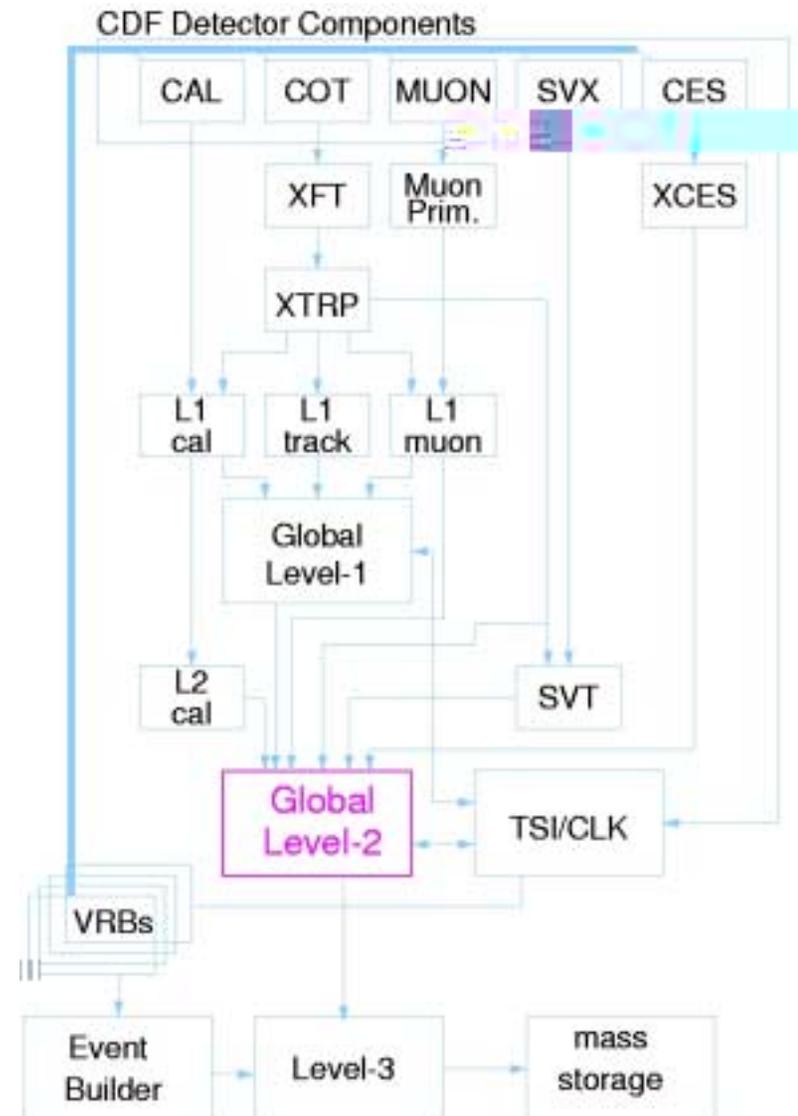




L2 Decision Crate Upgrade

Level 2 trigger receives information from:

- L1 trigger components
 - tracks, muons, jets, missing E_T , electrons
 - central strip chambers
 - silicon
- Information brought together and fed to processor(s) in the L2 decision crate
- L2 decision based upon trigger primitives
 - high rate (50kHz) in, must be fast





Run IIa Level 2 Decision Crate

- CDF Level 2 decision crate:
 - 7 different flavors of interface board
 - XTRP, SVT, L1, ISO, MUON, CES, Cluster
 - each uses different input format, different board designs
 - 1 board with Alpha processor for L2 processing/decision
 - system designed to run with 4 Alphas
 - diversity makes system challenging to test & maintain
- Current (in progress) CDF project to build a L2 trigger test-stand system (Pulsar project)
 - will have high speed I/O and buffering capabilities
 - system can source/sink data for **every** L2 interface board



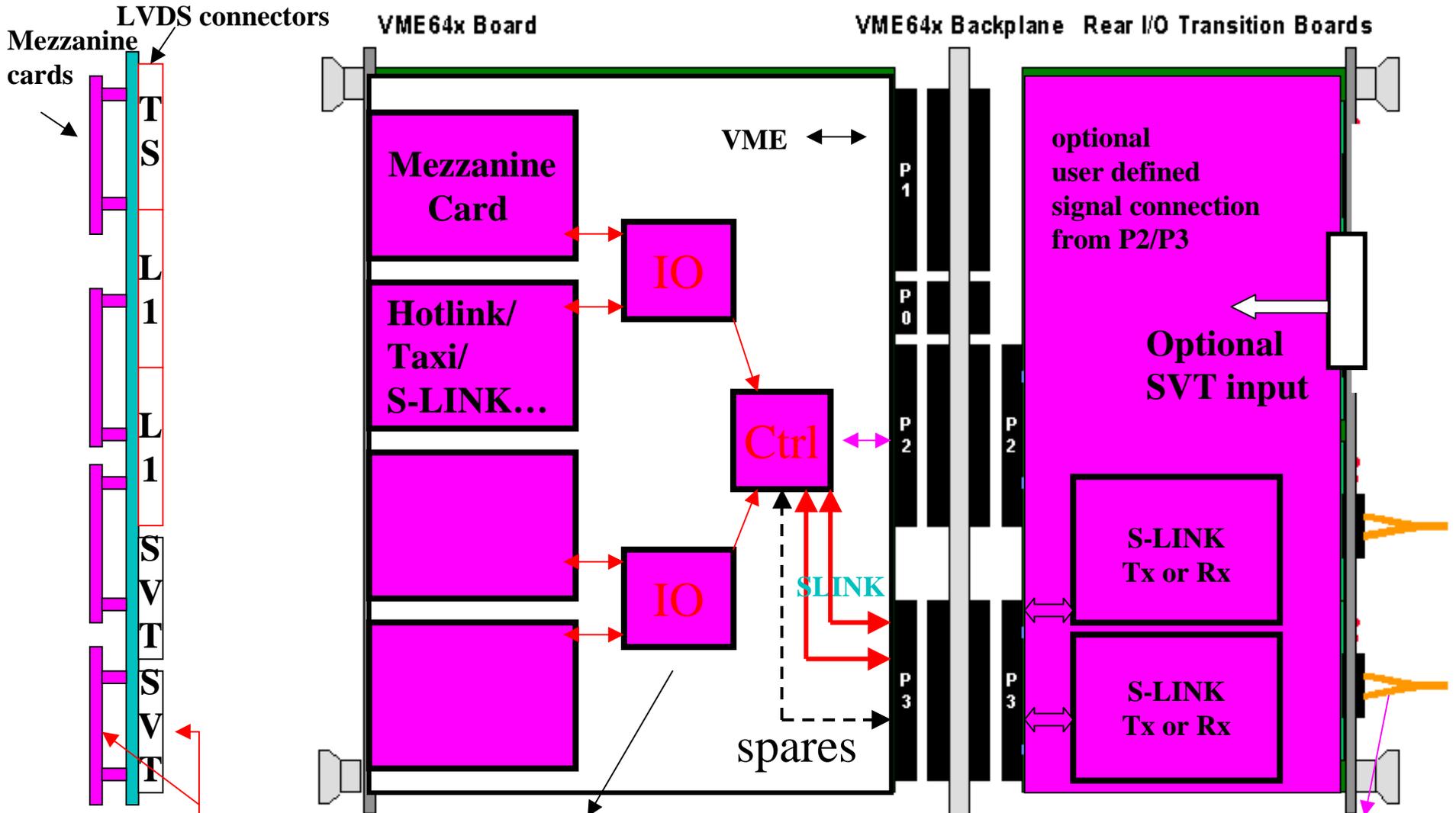
Level 2 Replacement

- DEC Alphas not feasible to maintain long term
 - no longer produced/supported.....DEC no longer exists
 - CDF internal review committee recommends replacing Alphas for Run IIb
- Concerns about long term operation & maintenance of large number of diverse interface boards
- **Replace existing L2 system with a Pulsar system**
 - interface board now common to every system
 - incorporates test/debug into interface board
 - data transfer uses S-link technology developed for LHC and supported at CERN
 - standard S-link ↔ PCI allows simple, high speed interface with commercial PC as L2 processor

Front-panel
(double width)

PULSAR design

Each mezzanine card can have up to 4 (hotlink/Taxi) fiber channels

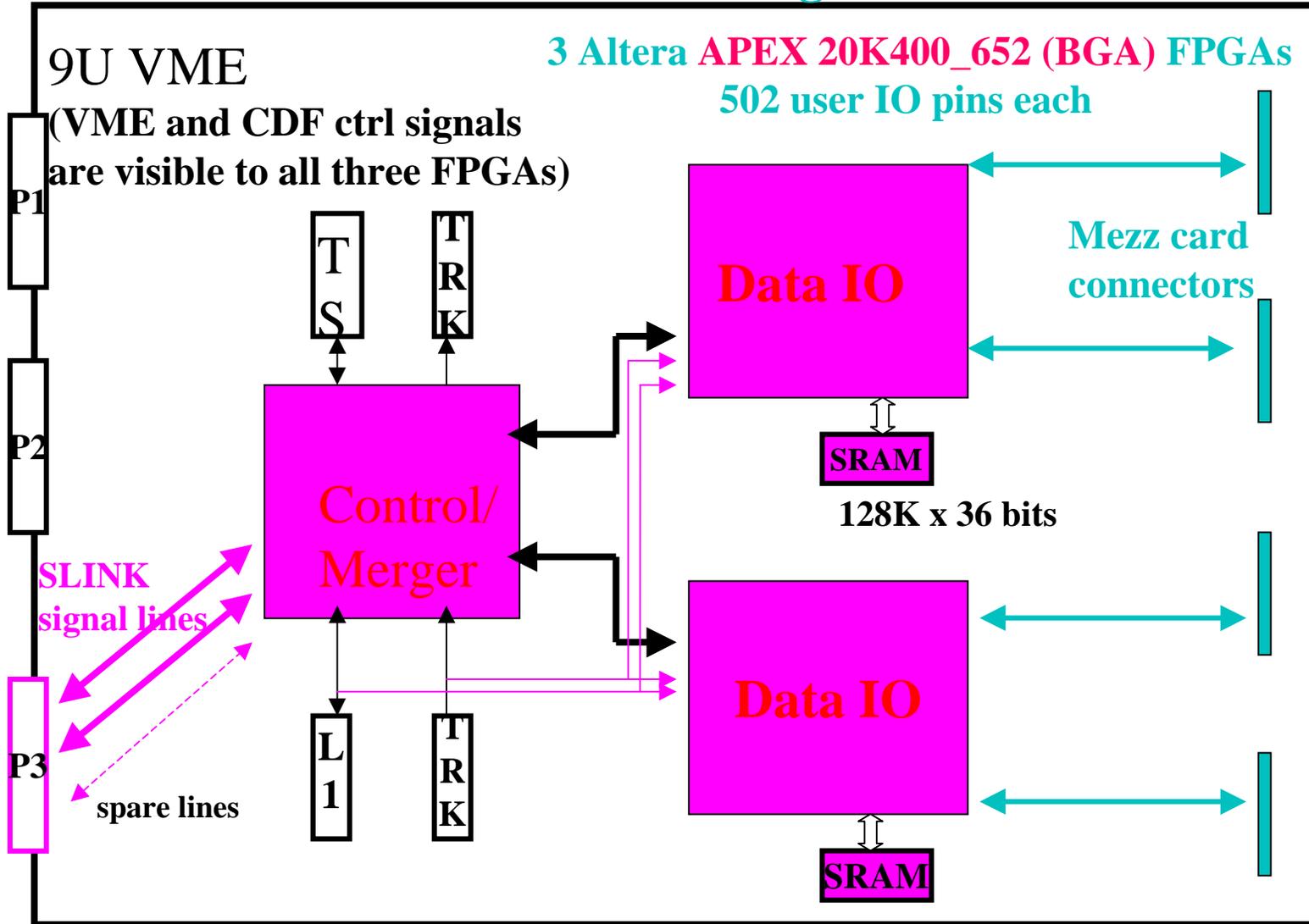


component side

Three FPGAs: Atera APEX20K400

The mezzanine card connectors can be used either for user I/O or SLINK cards

Pulsar design



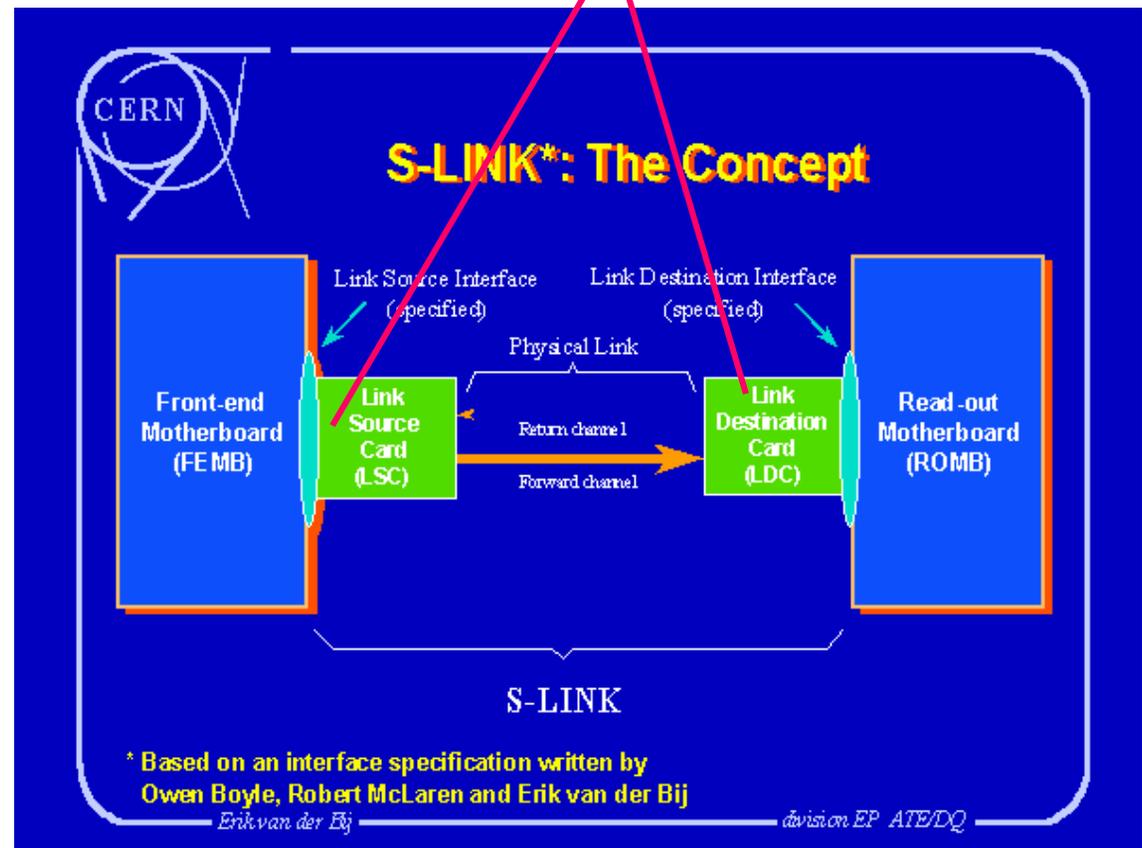
3 APEX20K400 FPGAs on board = 3 Million system gates/80KB RAM per board
2 128K x 36 pipelined SRAMs with No Bus Latency: 1 MB SRAM (~5ns access time)

SLINK format example:

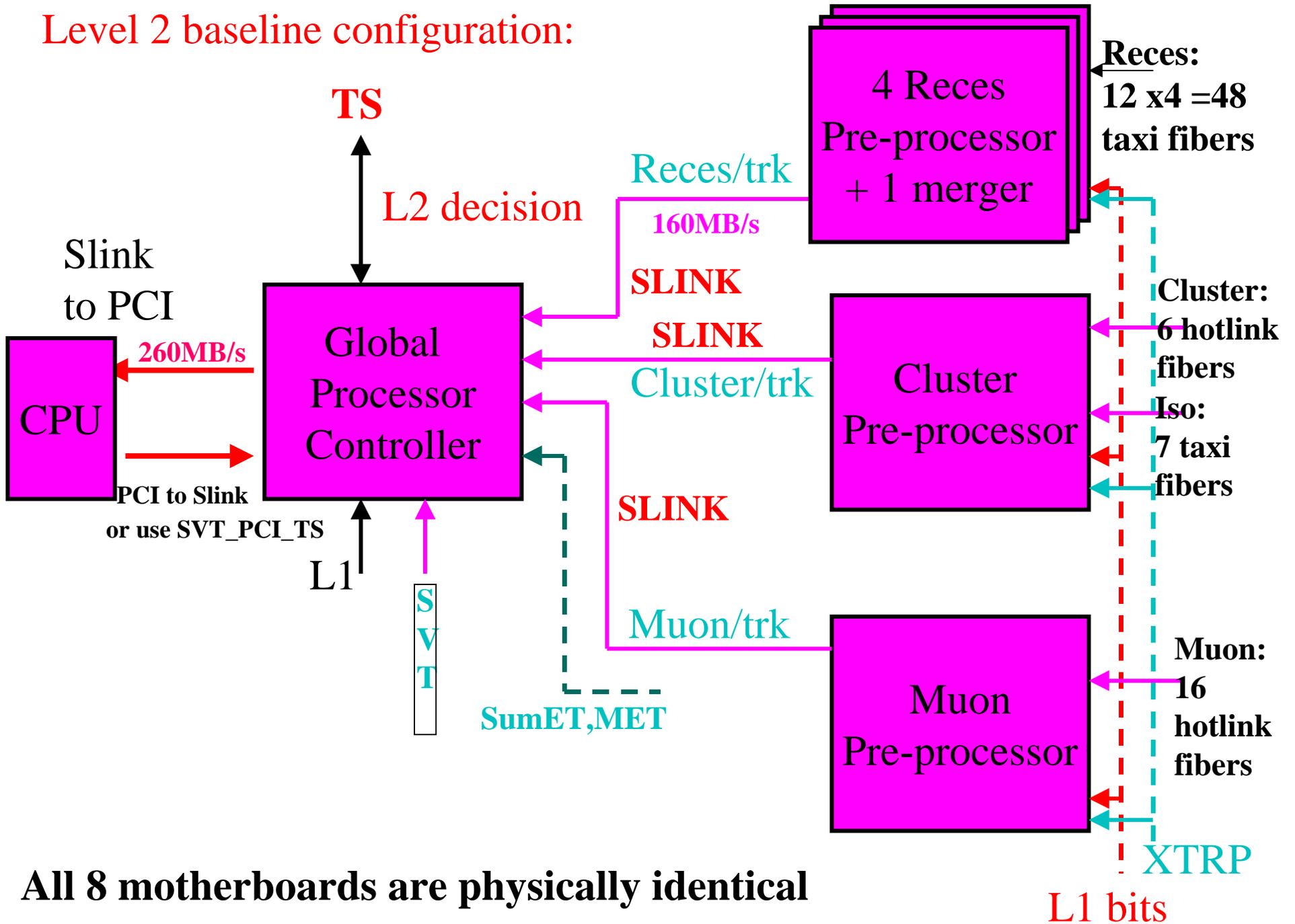
ATLAS SLINK data format

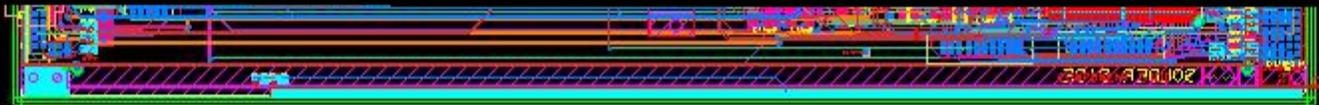
Beginning of Block control word
Start of Header Marker
Header Size
Format Version No.
Source Identifier
Level 1 ID
Bunch Crossing ID
Level 1 Trigger Type
Detector Event Type
Data or Status elements
Status or Data elements
Number of status elements
Number of data elements
Data/Status First Flag
End of Block control word

SLINK interface mezzanine card



Level 2 baseline configuration:



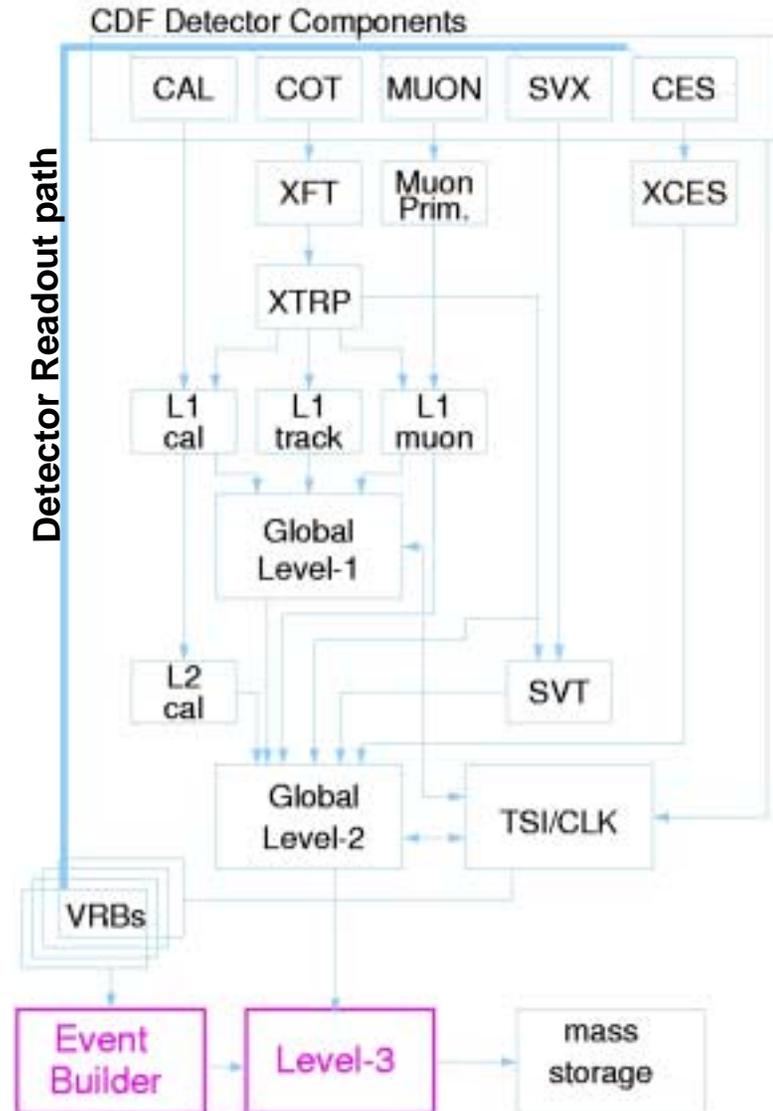




Event Builder/L3 Upgrade

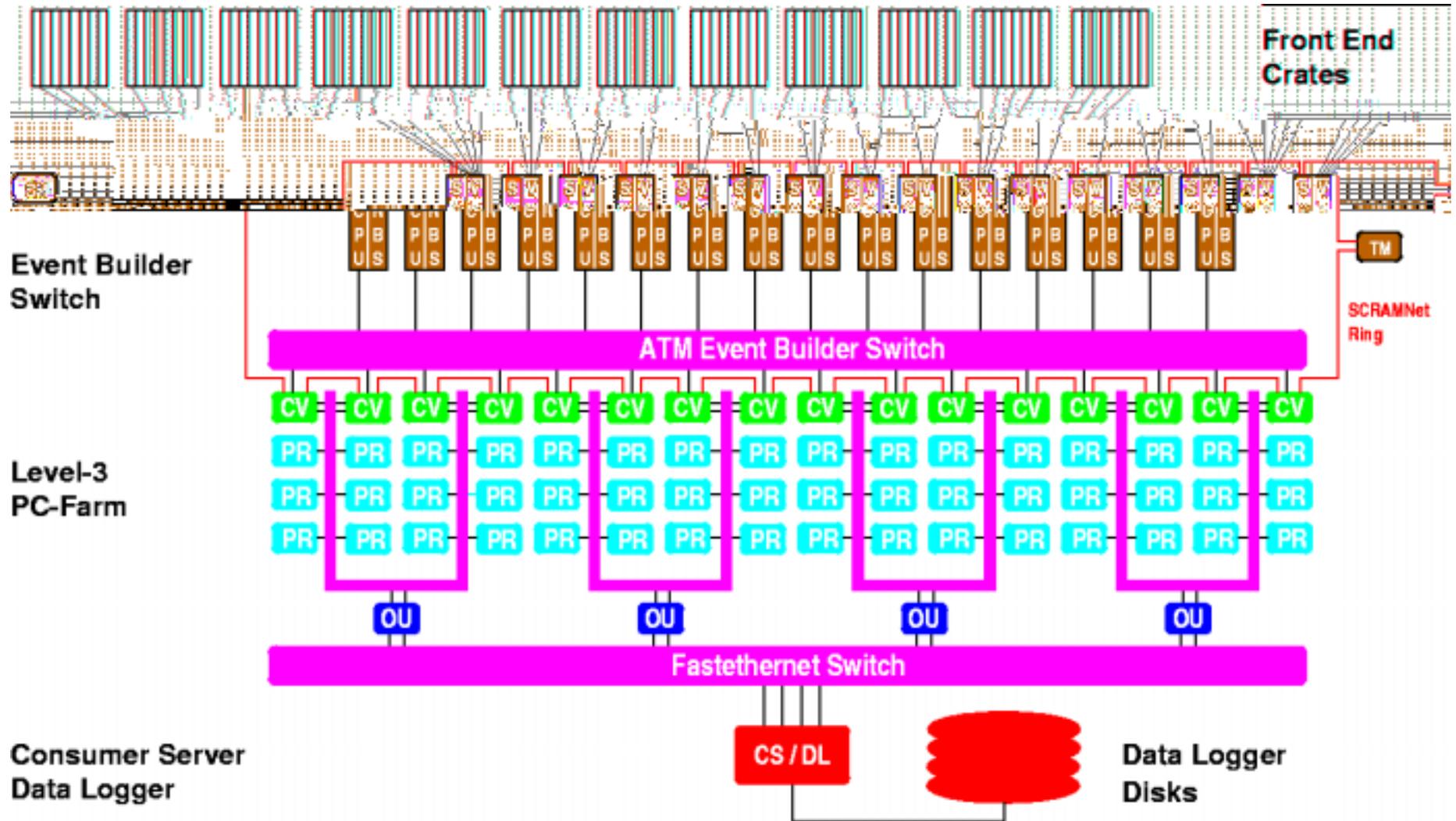
Full detector readout occurs on Level 2 trigger accept

- Event Builder
 - subsystems send data to VRBs
 - Event builder accepts data from VRBs, assembles the full event
- Level 3 Trigger
 - event sent: EVB→L3 PC farm
 - single PC node per event runs reconstruction & trigger algorithms
 - greater rejection at L3 needed in Run IIb





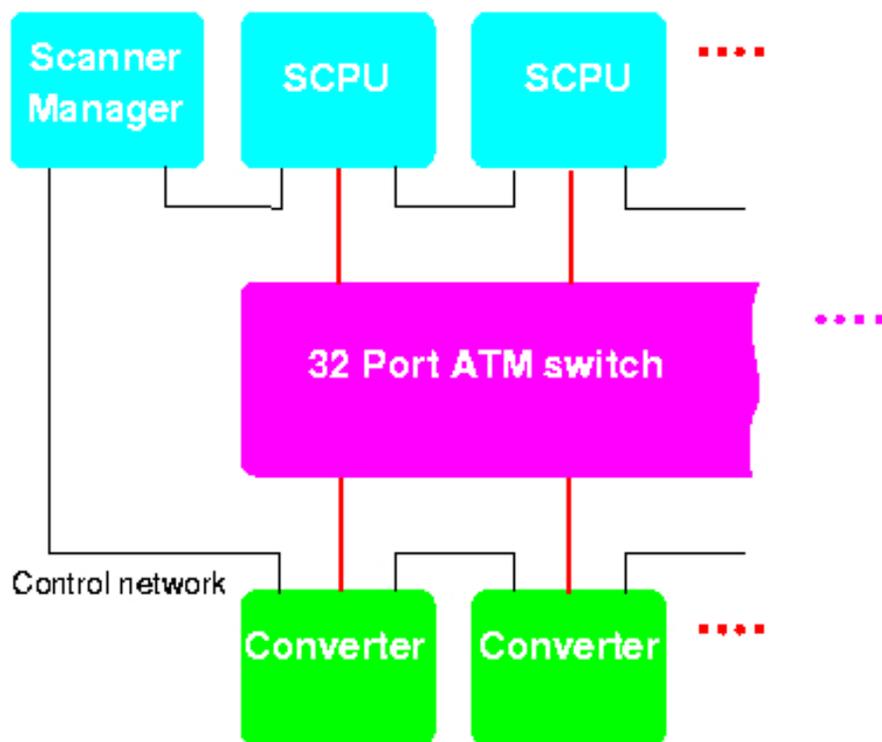
Readout/L3 Architecture



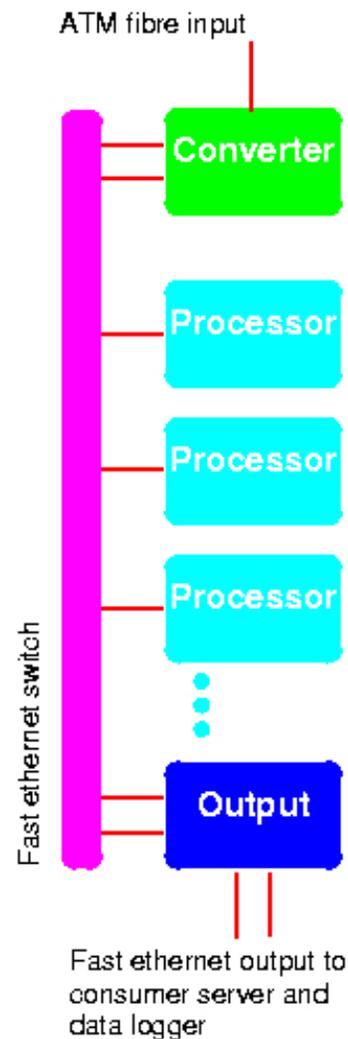


Readout/L3 Architecture

Event Builder Design



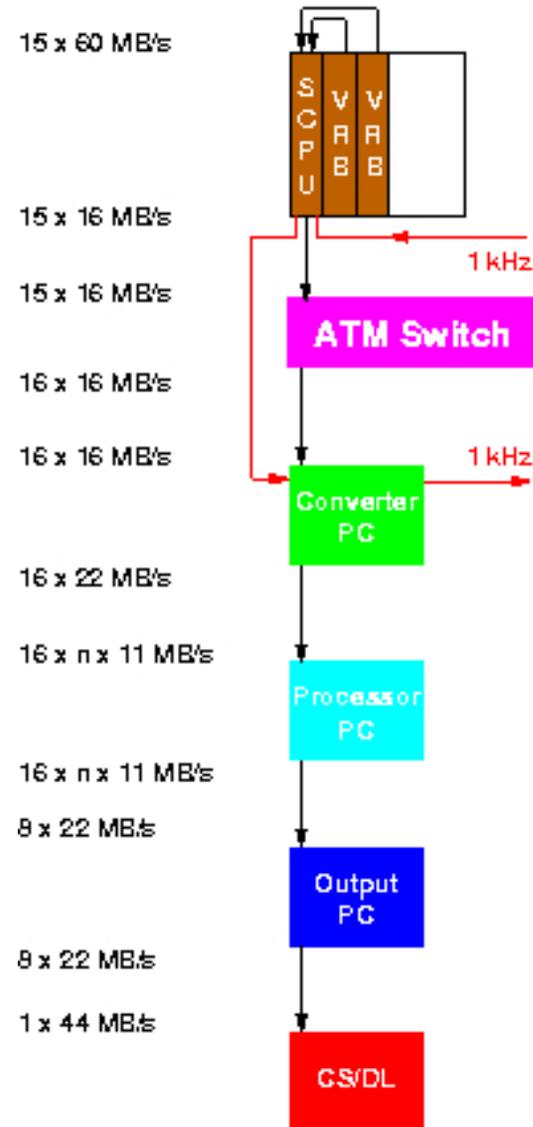
Level-3 Subfarm





ATM Upgrade

- Based upon Run IIb trigger table and data volume, extrapolate to ~400MB/s through ATM switch
 - current system ~240MB/s peak
- Upgrade system from ASX1000 ATM → ASX4000 ATM (bigger, newer, faster) going to OC12 ATM links
 - anticipate ~500MB/s or better





Level 3 PC Farm Upgrade

- More Level 3 PC processing power is required for Run IIb
 - reconstruction takes longer
 - higher occupancy
 - trigger algorithms more elaborate
 - greater rejection required

sample	Mean CPU time (seconds) [†]
t-tbar + 0 minimum bias	0.82±0.03
t-tbar + 5 minimum bias	2.66±0.10
t-tbar + 10 minimum bias	5.93±0.19
t-tbar + 15 minimum bias	8.32±0.67

[†] CPU time to run COT tracking on offline analysis computer (fcdsfgi2). Tracking code not optimized for higher luminosity conditions.

- Purchase processors at constant rate over 3 years of project
- Expect processor improvements will keep up with our growth in L3 needs throughout Run IIb
 - increased complexity of events offset by improved processing power



Trigger/DAQ Costs

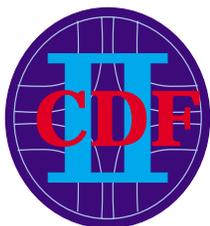
Total escalated cost + contingency:

<i>Fiscal Year</i>		2002	2003	2004	2005	2006	Totals
Escalation		1	1.021	1.046	1.076	1.106	
	<i>Total Base</i>	\$ 147,257	\$ 1,487,722	\$ 3,085,666	\$ 220,467	\$ -	\$ 4,941,113
	<i>Total Cont.</i>	\$ 112,290	\$ 967,515	\$ 1,480,906	\$ 77,614	\$ -	\$ 2,638,325
	<i>Total</i>	\$ 259,547	\$ 2,455,238	\$ 4,566,573	\$ 298,081	\$ -	\$ 7,579,439
	<i>R&D</i>	\$ 79,483	\$ 494,778	\$ 114,688	\$ -		\$ 688,949

M&S overhead 0.166

Labor overhead 0.29

includes G&A



Cost by Subproject

Costs listed in FY02 dollars:

WBS	Task Name	M&S	M&S cont.	Labor	Labor cont.	R&D	Total
1.3.1	Run 2b TDC Project	532,772	264,214	287,349	287,349	290,792	1,662,476
1.3.2	Run 2b Level 2 Project	215,419	64,626	17,680	8,840	0	306,565
1.3.3	Run 2b XFTII Project	1,011,934	505,967	544,032	272,016	313,418	2,647,367
1.3.4	Event-Builder Upgrade	414,000	124,200	0	0	0	538,200
1.3.5	Computers for L3 PC Farm	390,000	117,000	0	0	0	507,000
1.3.6	SVT Upgrade	294,000	294,000	0	0	0	588,000
1.3.	<i>Run 2b DAQ & Trigger</i>	2,858,125	1,370,007	849,061	568,205	604,210	6,249,608

These numbers do not include overhead or G&A

Comments:

- most of XFT labor is in the form of in-kind contributions from Ohio State, Illinois and Florida
- SVT labor included in M&S
- EVB/L3 labor all physicist manpower



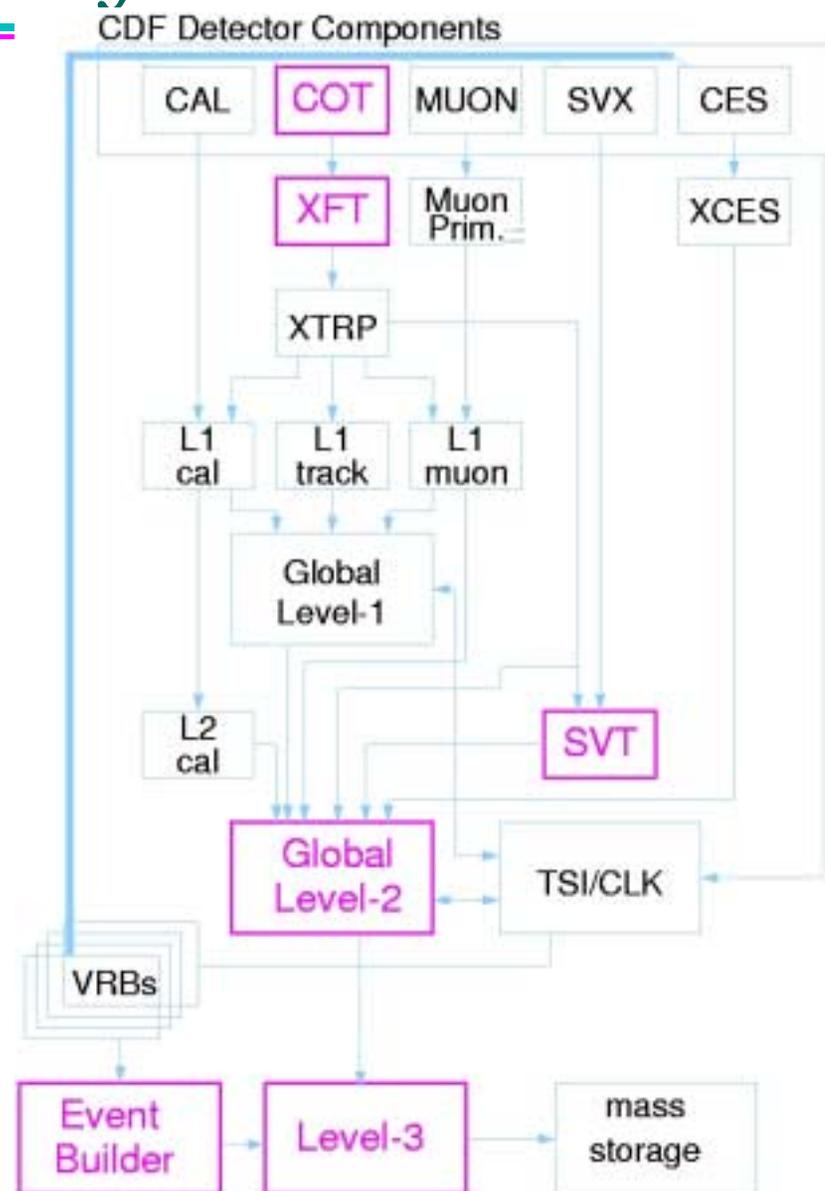
Project Schedule

- All components completed before silicon
- Preproduction complete, production well along (or complete) before shutdown for Run IIb
 - commissioning in full CDF system with beam
- Completion dates:
 - TDC 2/24/05
 - XFT 1/31/05
 - SVT 6/12/04
 - Level 2 9/09/04
 - EVB/L3 9/09/04



Summary

- These are the pieces of the CDF Front-end, Trigger and Data Acquisition system we need to upgrade/update to carry out a high p_T physics program
 - TDC replacement
 - XFT upgrade
 - SVT upgrade
 - L2 replacement
 - Event builder/L3 upgrade
- The remainder of the Run Iia CDF front-end/trigger/DAQ system will perform well throughout Run IIb





Supporting Documentation

- CDF Run IIb Technical Design Report
- “Report from the Run IIb Committee”
 - appendices: “Trigger Rates”, “XFT”, “Event Builder”, “TDC”
- CDF 6065: “COT Data Volume & Implications for Readout in Run IIb”
- CDF 5824: “A First Look at the Performance of the CDF Data Acquisition System”
- “Report from the TDC Review Committee”
- “CDF Run IIb TDC Specifications”
- CDF 5986: “Performance Study of the eXtremely Fast Tracker at High Luminosity”
- PULSAR Web page (documentation, schematics, BOM):
<http://hep.uchicago.edu/~thliu/projects/Pulsar>
- CDF 6059: “XFT Upgrade for Run IIb” CDF 6032: “Mezzanine Card Design Specifications for the PULSAR Board”