



Run IIb Silicon Upgrade: Technical Presentation

Baseline Readiness Review September 24, 2002

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For the CDF collaboration



Run IIb Silicon - Outline

- ◆ Overview of Goals and Constraints
- ◆ Layout
- ◆ Stave Concept
- ◆ Component Details
- ◆ L0 design
- ◆ Conclusions



Radiation Tolerance Implications

- ◆ In the fall 2000 a working group was formed to calculate the longevity of the IIa silicon detector
 - ➔ IIa cannot survive above $\sim 4 \text{ fb}^{-1}$
- ◆ Radiation damage consequences with the new detector:
 - ➔ Sensors should operate at high voltage ($\sim 350\text{V}$).
 - ➔ Sensors should be directly cooled ($\sim -5\text{C}$)
 - ➔ IC circuits in the detectors need higher level of radiation tolerance.
- ◆ To cope with higher doses during runIIb we need:
 - ➔ New readout chip (1/4um tech.)
 - ➔ Single sided sensors operating at high voltage
 - ➔ New H/L voltage distribution system
 - ➔ Need to directly cool the silicon
- ◆ Present technology allows all of the above to be achieved.

IIb conditions:

- ❖ $L = 2-4 \cdot 10^{32} \text{ cm}^{-2} \text{ sec}^{-1}$ at 396ns
- or $L = 5 \cdot 10^{32} \text{ cm}^{-2} \text{ sec}^{-1}$ at 132ns
- ❖ $\int L = 15 \text{ fb}^{-1}$

CDF RunIIa Silicon System Longevity		
	R(cm)	L (fb^{-1})
L00	1.3	7
L0	2.5	4
L1	4.1	8
L2	6.5	11
ISL	20-28	>40
DOIMs	14	6

Calculated Dose for lib Silicon		
Layer	Radius (cm)	Dose 10^{13} (1Mev neutron $\text{cm}^{-2} \text{ fb}$)
0	2.1	13.6
1	3.5	5.7
2	5.9	2.3
3	9.1	1.1
4	11.9	0.7
5	14.7	0.5



Silicon Upgrade for Run IIb

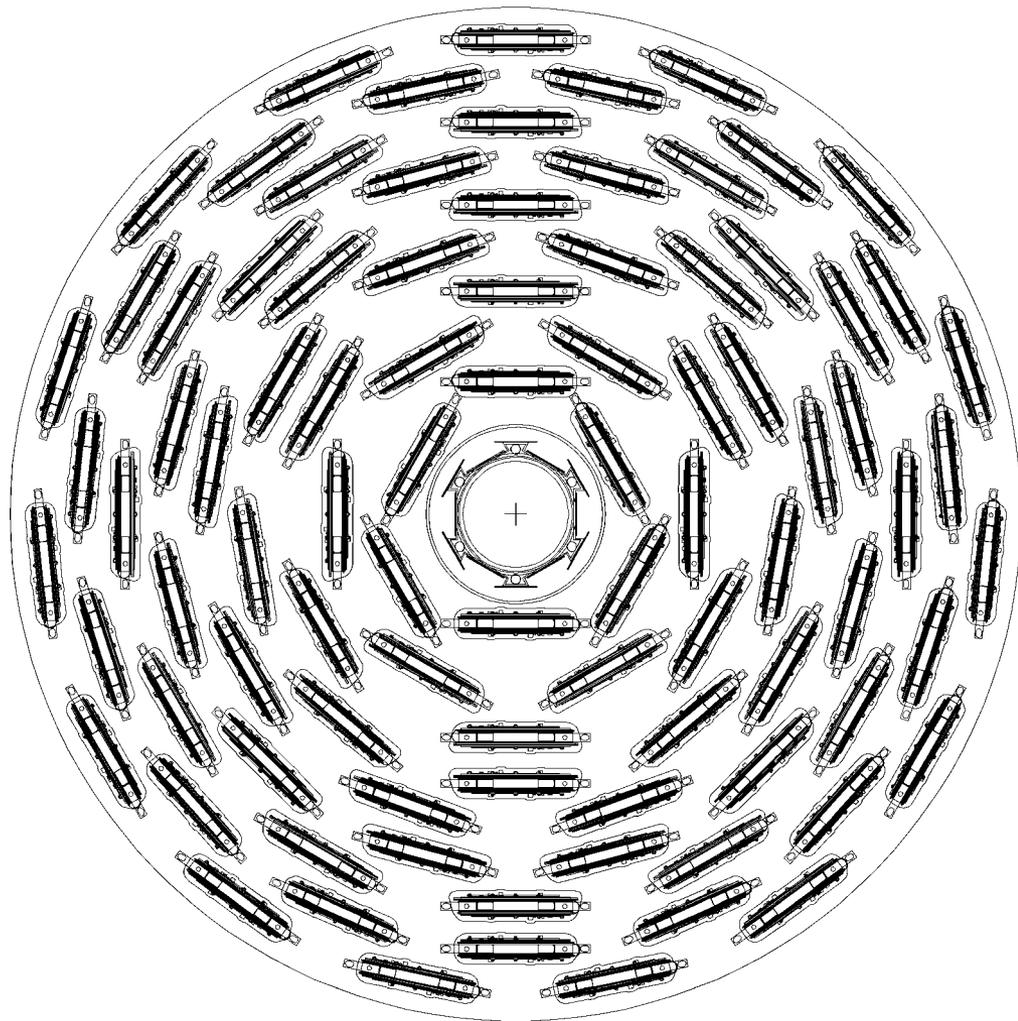
◆ Design Goals:

- ➔ Robust, simple, flexible and reliable design
- ➔ Minimize the cost
- ➔ Match or exceed performance of Run IIa silicon detector
- ➔ Minimize changes to infrastructure: DAQ or cooling systems
- ➔ Integrate CDF experience from SVX, SVX' and SVXII
- ➔ Pursue common solutions with D0:
 - **Svx4 chip**
 - **Technology of silicon**
 - **Direct cooling**
 - **Hybrid technology**
 - **L0 technology**



RunIIb Layout

- ◆ Final layout choices are the results of many internal reviews with inputs also from Laboratory committees.
- ◆ Main Layout Choices:
 - ➔ 6-fold symmetry
 - ➔ 1 stave design for all 5 outer layers
 - ➔ Fill all space available up to ISL
 - ➔ Maximum flexibility in the choice of Axial/Stereo layers
 - ➔ Innermost layer (L0) similar to the present L00





Run IIb Layout Details

Layer	Fold	Type	Radius (mm.)	pitch/RO (um)	angle	Sensors	Hybrids	#chips
0	12	Axial	21.0 and 25.0	50/25	0	144	72	144
1	6	Axial	35.5 and 43.5	75/37.5	0	72	36	144
1	6	Axial	40.0 and 48.0	75/37.5	0	72	36	144
2	12	Axial	59.5 and 74.75	75/37.5	0	144	72	288
2	12	Stereo	64.0 and 79.25	80/40	1.2	144	72	288
3	18	Stereo	90.75 and 104.5	80/40	1.2	216	108	432
3	18	Axial	95.25 and 109.0	75/37.5	0	216	108	432
4	24	Stereo	119.25 and 133.0	80/40	1.2	288	144	576
4	24	Axial	123.75 and 137.5	75/37.5	0	288	144	576
5	30	Axial	147.5 and 161.5	75/37.5	0	360	180	720
5	30	Axial	152.0 and 166.0	75/37.5	0	360	180	720
Totals						2304	1152	4464
Totals SVXII + L00						864	768	3276
Total Increase						267%	150%	136%
% outer layers						94%	94%	97%

94% of sensors and hybrids are 4-chip



RunIIb Layout

- ◆ Emphasis on simplicity and flexibility
- ◆ Easy to be mass produced
- ◆ Minimum number of parts:
 - ➔ 1 hybrid (4 chips)
 - ➔ 2 sensors (axial and stereo)

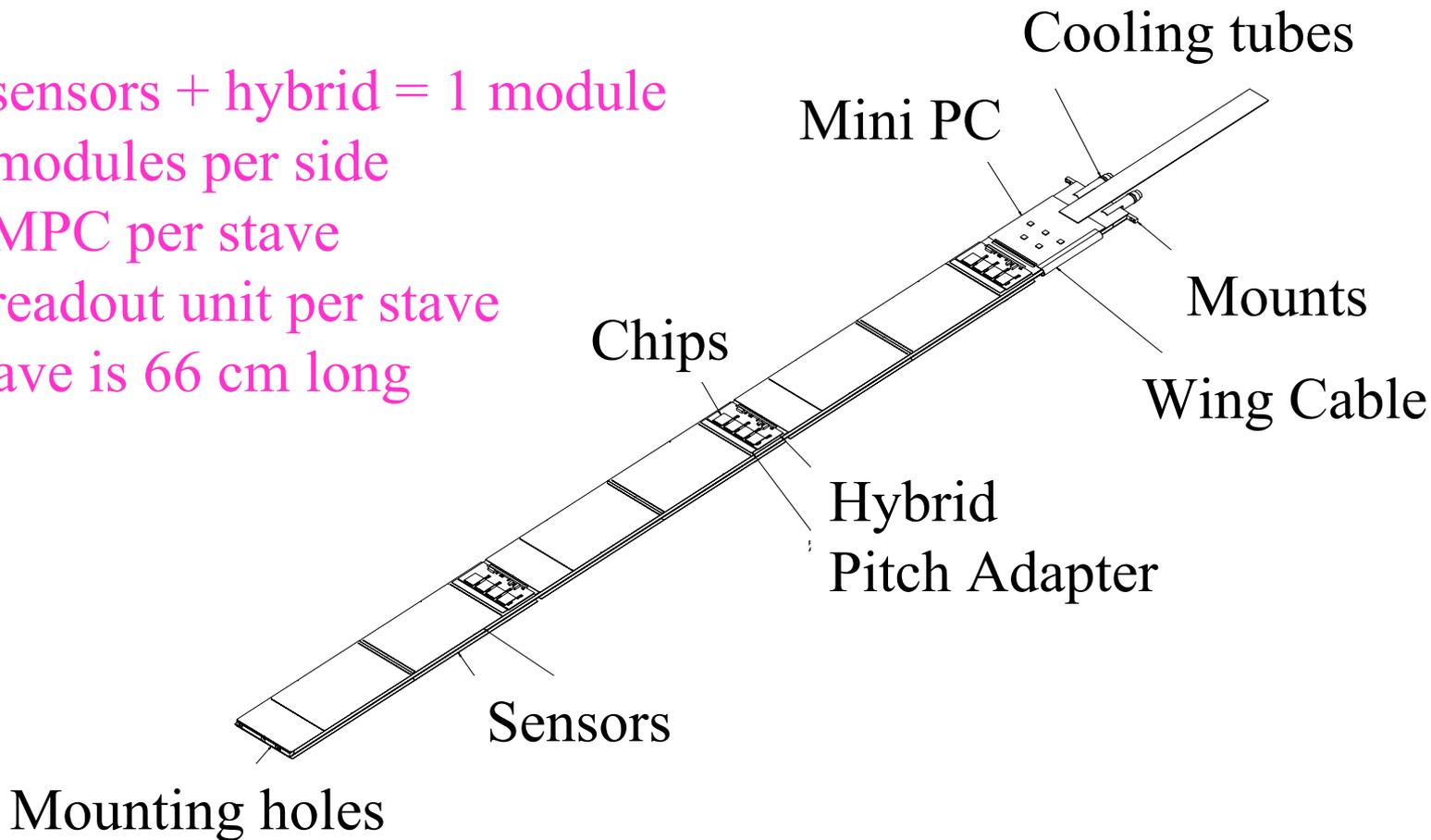
parts	SVXIIa	SVXIIb
hybrids	10	1
sensors	5	2
ladders	5	1

- Single stave design:
 - ➔ Minimize R&D
 - ➔ Minimize tooling
 - ➔ Minimize production time
- Carbon fiber bulk-heads with inserts for precision alignment of staves



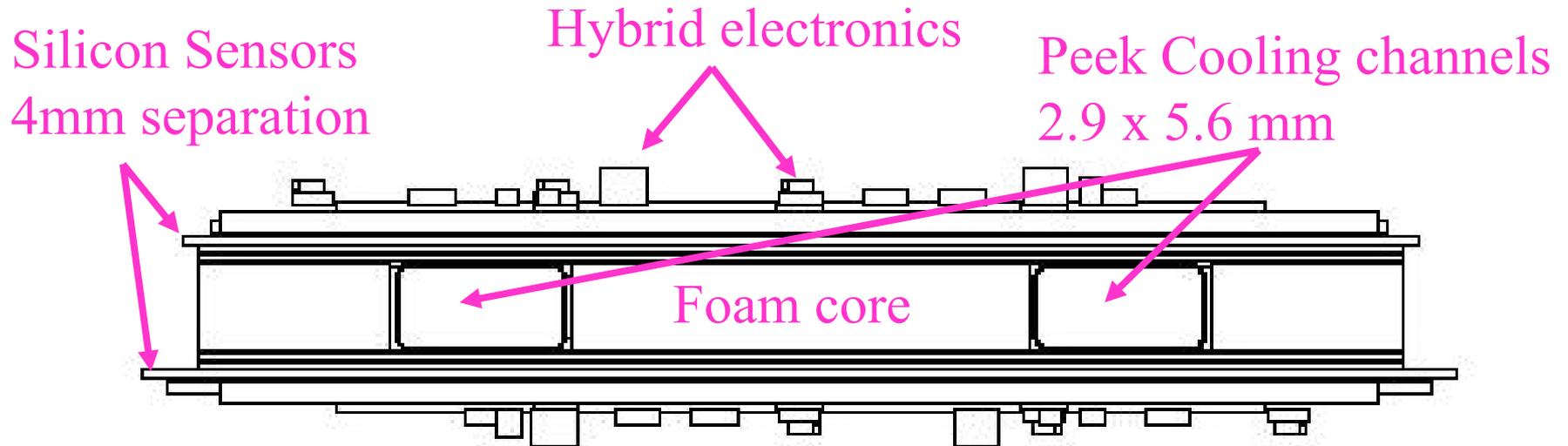
Stave: conceptual view

- 2 sensors + hybrid = 1 module
- 3 modules per side
- 1 MPC per stave
- 1 readout unit per stave
- Stave is 66 cm long





Stave: end view



Material/stave:

- 1.8% RL
- 124 grams

Fraction of Total RL:

- Sensors 39%
- Hybrids 13%
- Bus Cable 17%
- CF/Coolant 29%



Stave: cooling issues

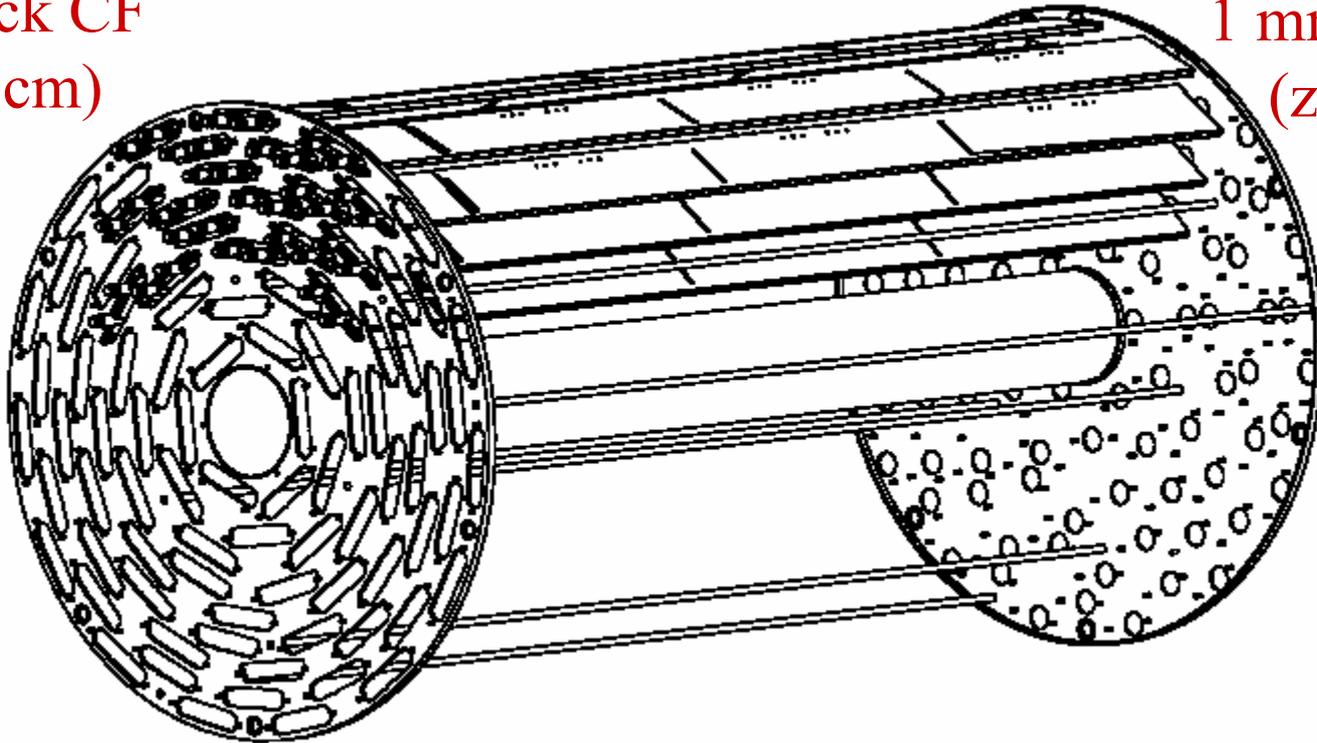
- ◆ Temperature specs for silicon:
 - ➔ Keep silicon cool to limit the amount of noise increase due to leakage current and limit the reverse annealing effect
 - ➔ Studies of these effects set temperature limits:
 - Layers 4-5: $T < 15^{\circ} \text{C}$
 - Layers 2 and 3: $T < 10^{\circ} \text{C}$
 - Layers 0 and 1: $T < -5^{\circ} \text{C}$
 - ➔ Requires active cooling of silicon
- ◆ Stave design incorporates cooling tubes (Peek) which meet specs
- ◆ Total heat load very similar to Run Iia $\sim 3\text{KW}$
- ◆ Plan to use existing cooling system with increased glycol concentration (43%) for operation at -15°C



Barrel assembly

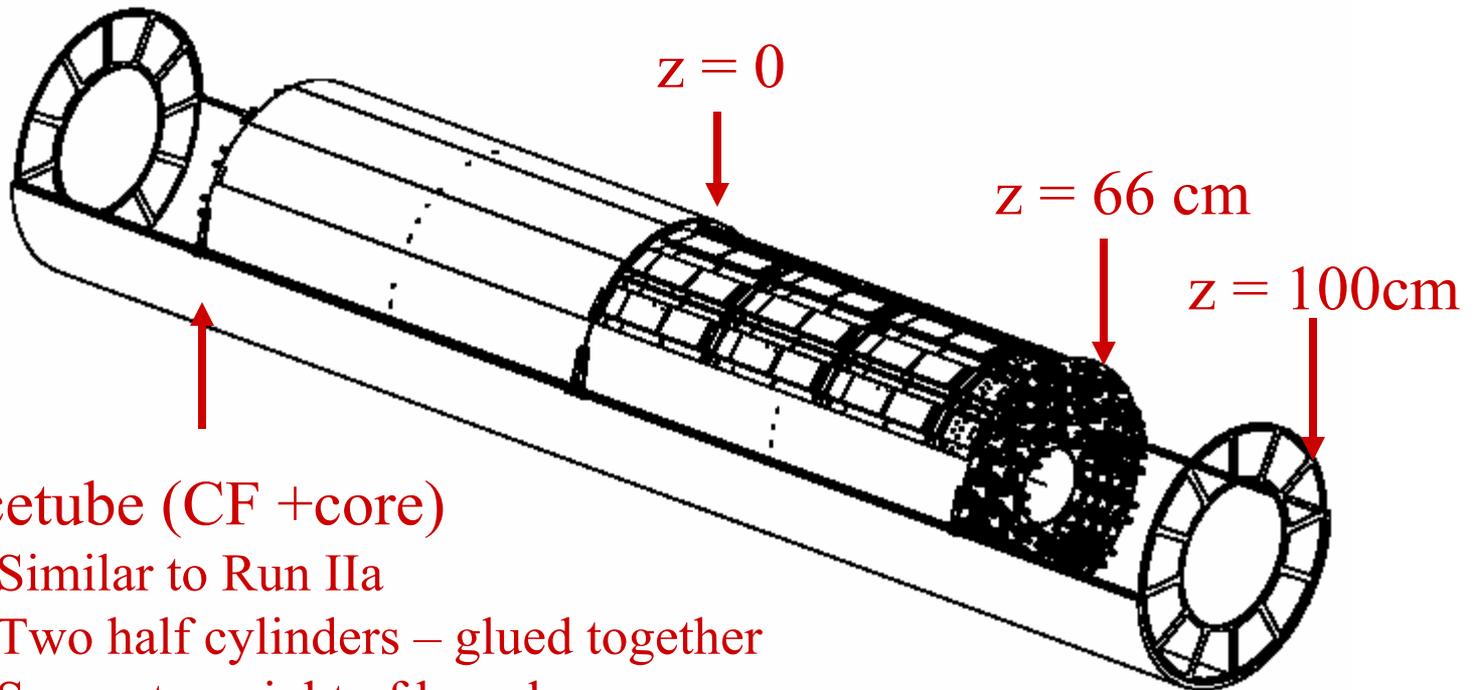
Outer Bulkhead
2 mm thick CF
($z = 66$ cm)

Inner Bulkhead
1 mm thick CF
($z = 0$ cm)





Barrel in Spacetube



Spacetube (CF + core)

- Similar to Run IIa
- Two half cylinders – glued together
- Supports weight of barrels
- Attaches to mount points on ISL end flanges



Layer 0 Design

- ◆ Inner Layer (L0) follows Run IIa L00 design:
 - ➔ Smallest possible pitch – 25/50 micron pitch
 - ➔ Fine pitch cables connect sensors to hybrids
 - ➔ Hybrids are located out of tracking volume ($\sim z=70\text{cm}$)
 - ➔ Positioned at small radius (2.1 cm)
 - ➔ Hybrids \sim similar to outer layer, but 2 chips
 - ➔ Will be supported by outer barrel (not beampipe)
- ◆ Low mass construction is of utmost importance for 1st measurement
- ◆ Sensors are identical to L00 sensors
- ◆ Cables:
 - ➔ All cables designed and the longest has been fabricated by KeyCom (Japan)
 - ➔ Some technical issues with the L0 cable sorted out BUT yield must be improved
 - ➔ We are pursuing other possible vendors with also the option of splicing the cable.



L0 Layout

Fine pitch cables

- Max. length 59cm
- 100um pitch
- 50um pitch at ends

Hybrids

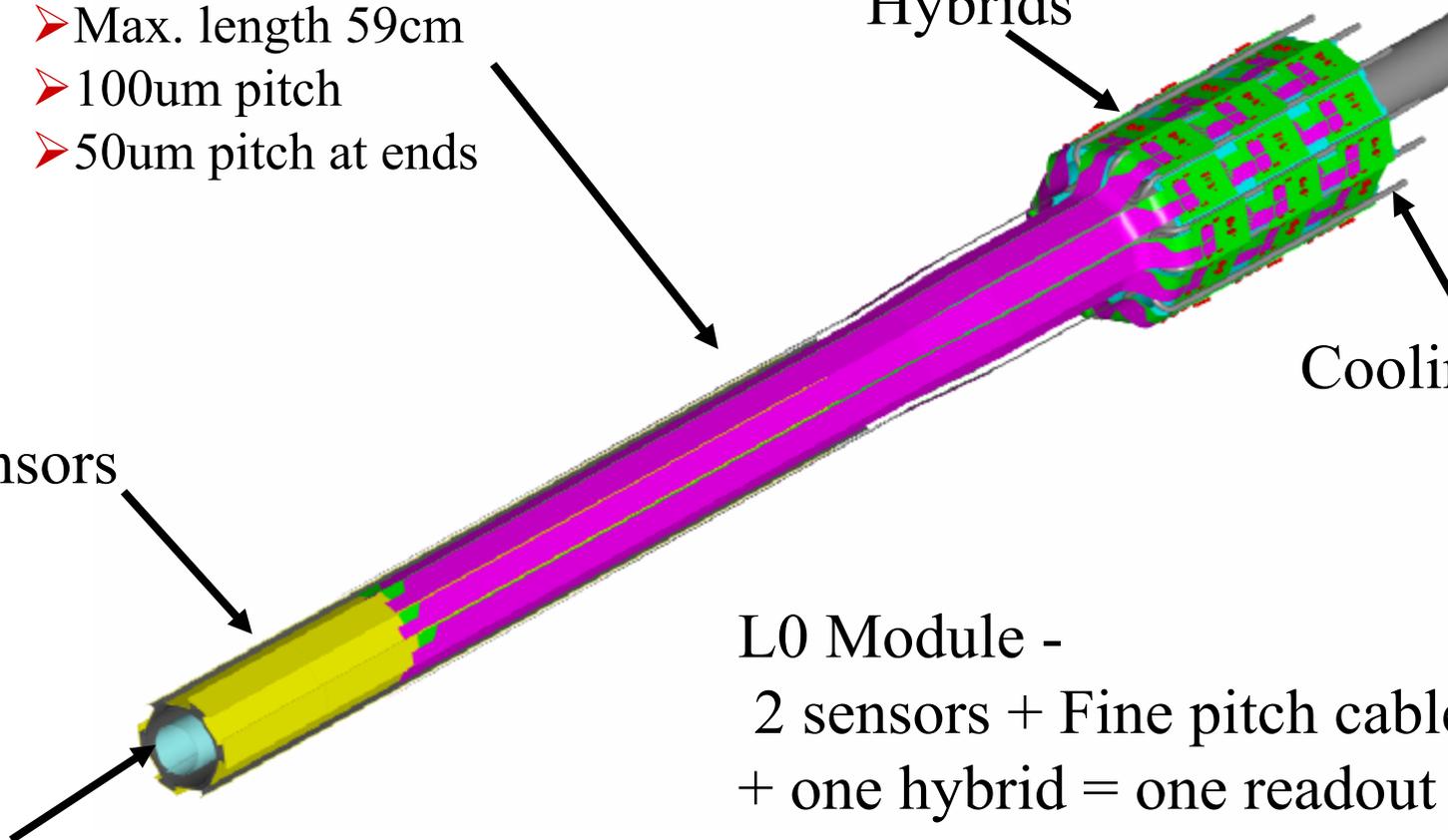
Cooling tubes

Sensors

L0 Module -

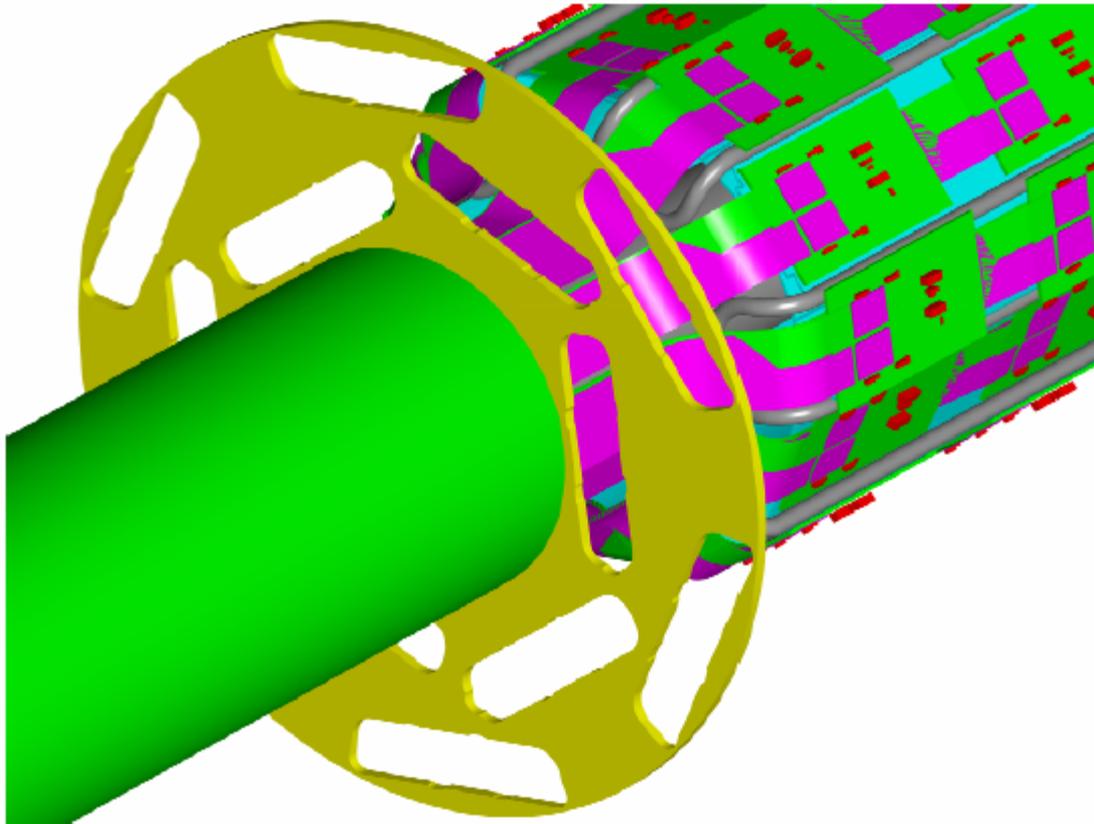
2 sensors + Fine pitch cables
+ one hybrid = one readout unit

Beampipe and CF support





L0 hybrids and cables



Cable flare out in radius (to $\sim 4\text{cm}$) after passing through bulkhead

Cables from successive modules pass underneath hybrids from lower z modules

Cooling tubes integrated into hybrid support structure



Run IIb Status –outer layers

- ◆ Our r&d effort pivots on the stave tests
- ◆ All stave prototype parts are in hand:
 - Prototype sensors
 - Prototype Hybrids
 - Prototype module fixtures are ready and tested
 - Prototype Bus cables
 - PCB version of the mini Port Card (BeO version expected at the end of September)
 - Prototype stave cores
 - Test Stands (= final DAQ system) are ready and used for testing
- ◆ Main point is to verify the noise coupling between the Silicon and the Bus Cable.
- ◆ **Expecting results in late October**

2 Prototype modules built (9/13)



Silicon Sensors

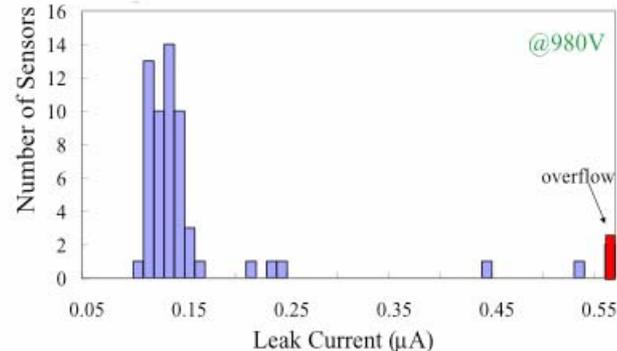
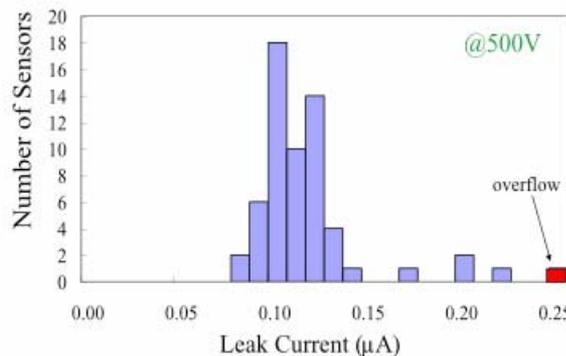
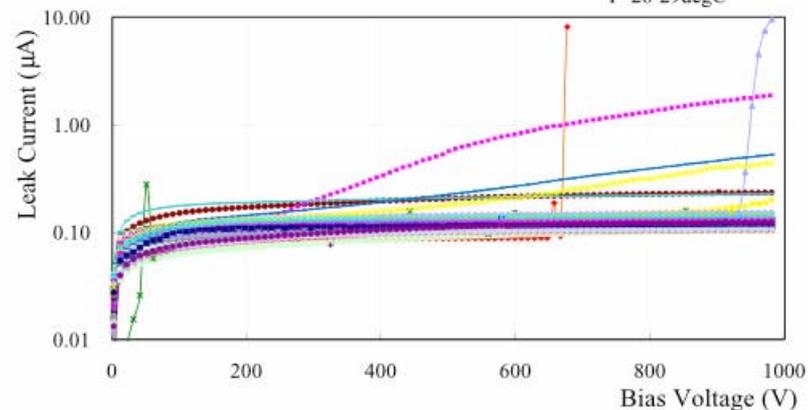
All detectors are single sided and based on the high voltage operation layout (CMS, ATLAS, L00)

- Easy to build, test and handle
- Minimal R&D necessary
- Prototype (identical to final sensors) already in hand
- High yield and high quality (0% bad channels grade “A” and 0.07% grade “B”)
- Full characterization in progress (radiation damage studies in early October)

SVX2b Outer Axial Sensors (Hamamatsu Photonics)

2002.7.16
T=28-29degC

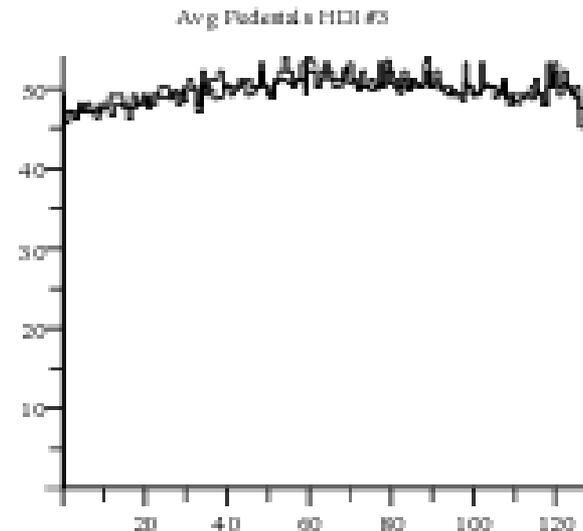
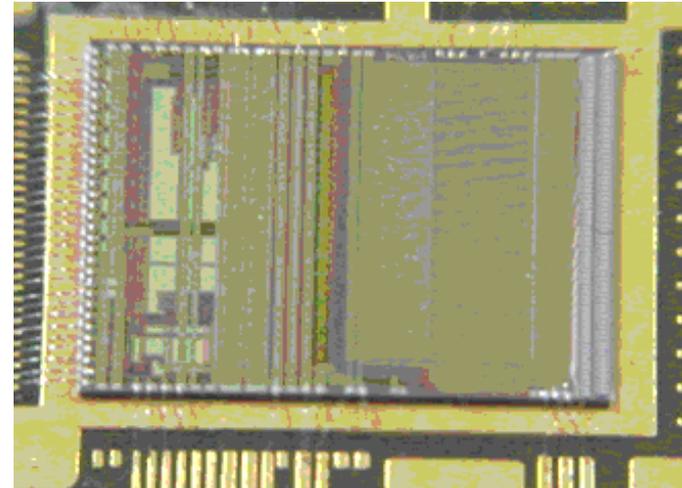
I-V curves of 60 prototypes, measured by U Tsukuba





SVX4 chip

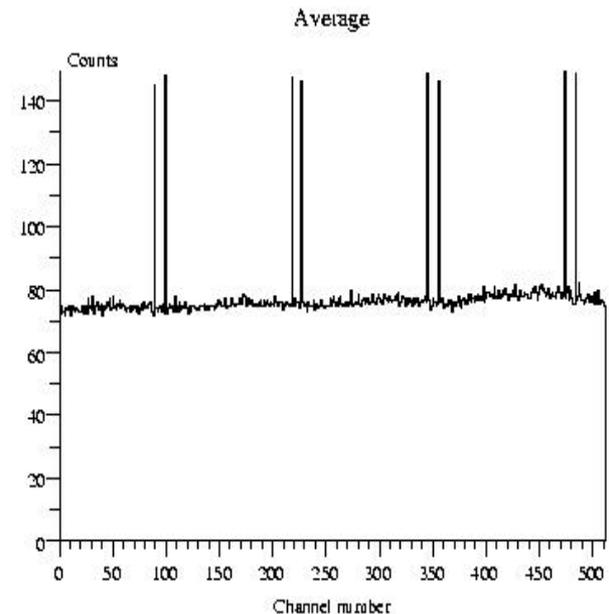
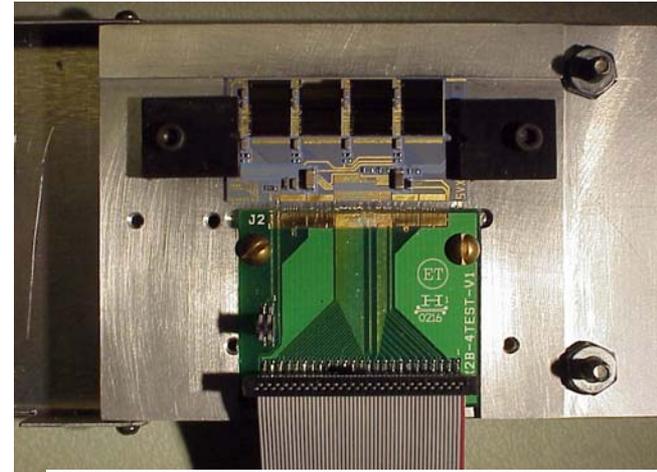
- ◆ It is a 0.25um translation of the SVX3d chip
- ◆ Design started in fall 2000 as a collaboration between LBL, FNAL and INFN-Padova. B.Krieger (LBL) lead engineer.
- ◆ 1st full prototype submission in April '02
- ◆ Chip back in June '02
 - ➔ Tested both at LBL and FNAL
 - ➔ No major problems found (so far)
 - ➔ Some adjustment required to meet production quality





Hybrids

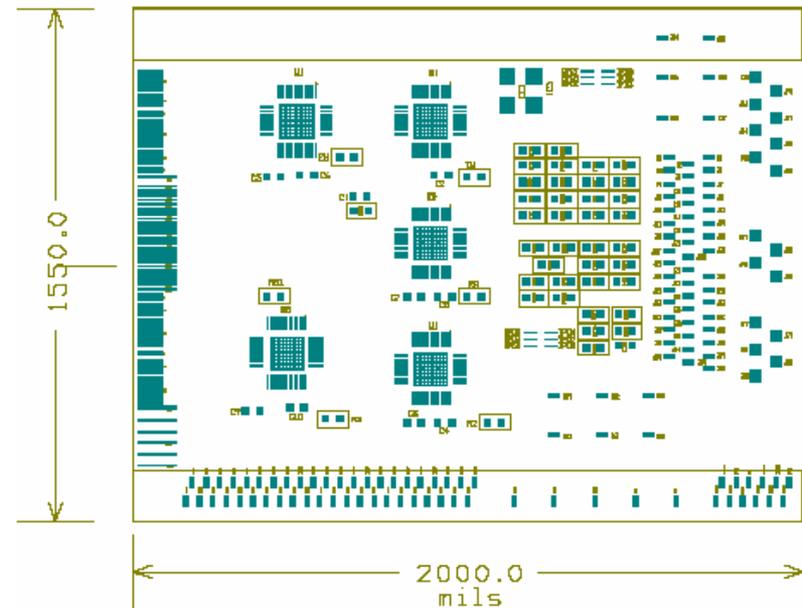
- ◆ Hybrids are fabricated on a Beryllium Oxide substrate for improved thermal performance and long radiation length.
- ◆ Hybrid layout uses advanced fine pitch technology for reduced area.
- ◆ Integrate SVX-II (a) experience into design, materials choices, and components to enhance reliability and simplify fabrication, assembly, and test.
- ◆ Hybrid appears to work with no apparent problem seen yet.
- ◆ **SVX4 chip performance on hybrid same as single chip on test board.**





Mini Port Card

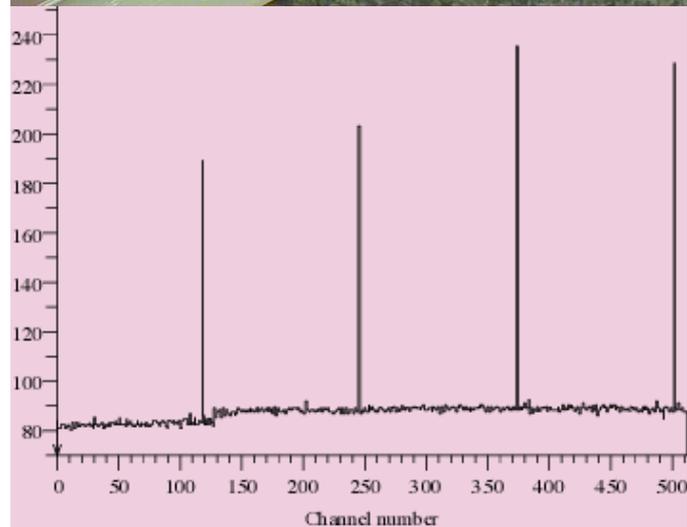
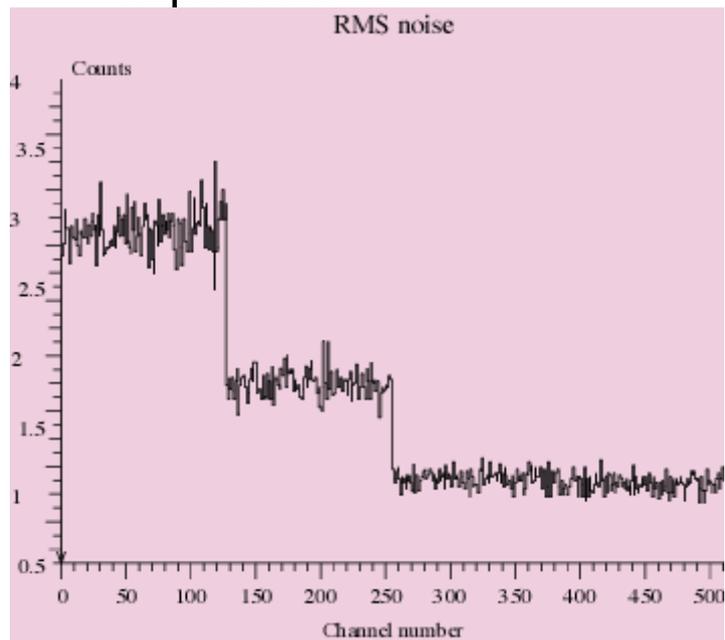
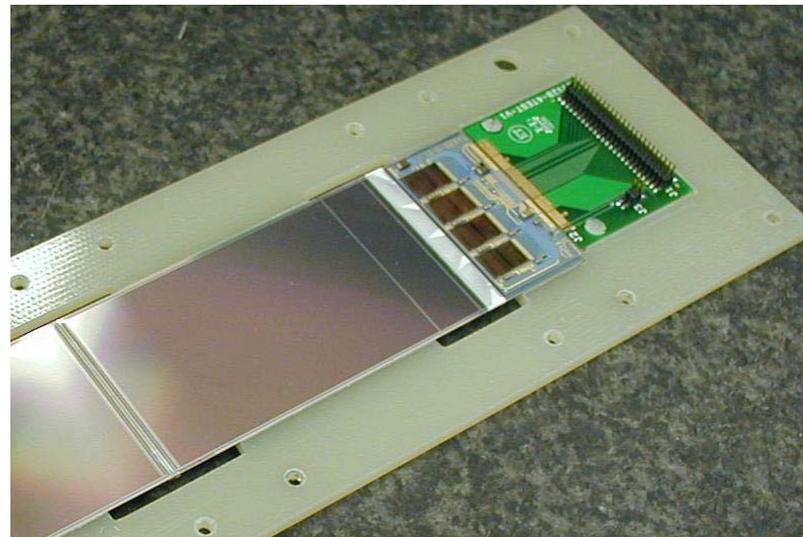
- ◆ Uses the same BeO substrate as the hybrid
- ◆ Connects to the top and bottom bus cable (directly and via a foldable “wing” cable)
- ◆ Controls all data, commands and power going in/out of the stave
- ◆ An FR4 version has been produced to allow start of electrical stave tests.
- ◆ BeO prototype expected by end of September
- ◆ 5 transceiver chips are mounted for data control
- ◆ Transceiver:
 - ➔ A new (0.25um) transceiver chip has been designed and submitted to MOSIS
 - ➔ New transceiver simplifies connectivity and eliminates the need for an extra power line
 - ➔ New transceiver fits in the silicon space left over by the svx4 chip
 - ➔ MPC is also compatible with the old transceiver which we have already plenty left over from IIa





Module

- ◆ First two modules fully assembled
- ◆ Mechanical procedures are satisfactory
- ◆ Preliminary results confirm our expectations.





Summary of Run IIb design

- ◆ New naturally Radiation hard chip required for Run IIb luminosity.
 - Prototype is in hand and functioning well!
- ◆ DAQ simplified wrt Run IIa
 - No optical components
 - New Power Supplies: off-the-shelf, not custom
 - Number of readout chains (252) much lower than available in existing infrastructure (408): more spare parts will be available !
- ◆ Uniform stave design for $\sim 94\%$ of the detector
 - Only one type of fixturing to develop for outer layers
 - L0 ~ L00 type construction
- ◆ Small number of different style parts
 - Only 2 types of hybrids – 4 chip on outer layers, 2 chip on Layer 0
 - L1-5 have 2 sensor types (axial and small angle)
 - L0 sensors = L00 sensors.



Conclusions

- ◆ Great effort put into design simplification, ease of construction and low risk technology
- ◆ Design relies heavily on experience with previous silicon detectors at CDF (SVX, SVX', SVXIIa, L00 and ISL)
- ◆ We expect the total mass in the tracking volume to be below the present value in spite of the increased number of sensors and need for direct cooling
- ◆ DAQ simplified, active components are more accessible
- ◆ All prototype parts are in hand and testing is under way
- ◆ Preliminary test results agree with expectations!