CDF Run IIB Silicon Upgrade

Technical Design Review

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Fermilab

For the CDF Collaboration

Run 2b Silicon Technical Design

- ð Goals and Constraints
- ð Layout: changes since TDR
- ð Stave Concept
- ð Component Details
- ð Cooling Studies
- ð Material and Stiffness
- ð Descoping (effect of dropping a layer)
- ð Conclusions

- Note: Additional mechanical and simulation studies may result in some changes in the layout, but these changes will be motivated by simplification and will not increase the scope of the project.

Run IIB

Lab plans to run through 2007, with 6m shutdown starting Jan. 2005

Year	# months	L_{cum} (fb^{-1})	L ($cm^{-2}s^{-1}$)	Comment
2001	8	0.2	$3\ 10^{31}$	
2002	10	1	$8\ 10^{31}$	
2003	8	2.0	$1.2\ 10^{32}$	go to 132 ns
2004	11	3.8	$2\ 10^{32}$	Numi starts operating
2005	8	6.3	$4\ 10^{32}$	
2006	11	10.7	$5\ 10^{32}$	
2007	10	14.7	$5\ 10^{32}$	

Run IIB working group found that L00 and SVXII will survive to ~ 4 fb^{-1}:

CDF	R_{min} (cm)	L (fb^{-1})
L00	1.35	7.4
L0	2.54	4.3
L1	4.12	8.5
L2	6.52	10.7
ISL	20 - 28	>40
DOIMs	14	5.7

- RunIIb Working Group report used Run1a and Run1b data to estimate lifetime of Run2a detector.
- Run 2a is instrumented with 144 TLDs on SVXII outer shell and Plug face
- Preliminary results (Oct. 30th!) confirm WG assumptions on radial dependence of dose → Current detector will survive until the shutdown
- Studies and analysis of TLD data will continue

Radiation Dose Measured Run IIA

May – Oct running

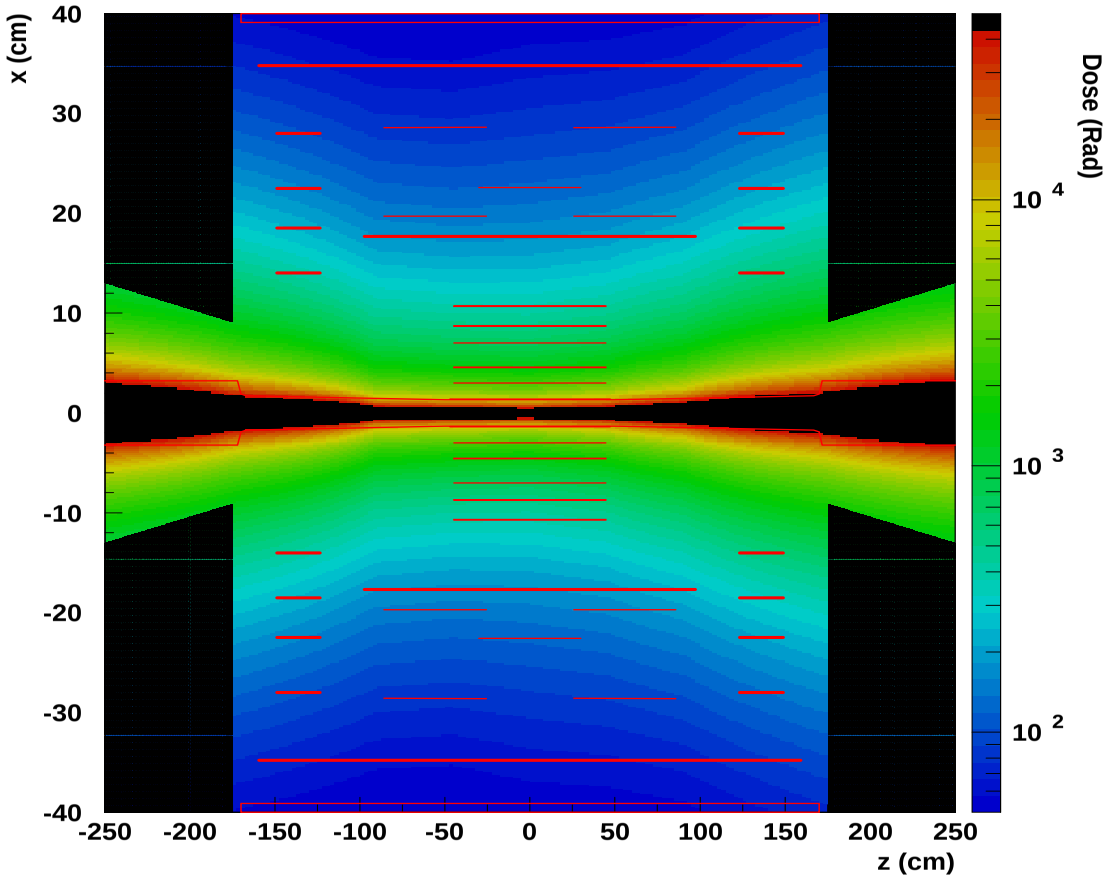
Collision dominated, but losses still present

Measurements found radial and z dependence of dose

Radial dependence fit to $1/R^{\alpha}$ scaling

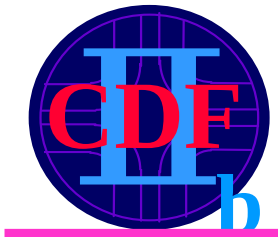
$\alpha = 1.6\text{-}1.7$

Run IIA lifetime estimates assumed $1.5 \pm 30\%$



Radiation Tolerance Implications

- SVXII double sided silicon limited in bias voltage
  - ð Need single sided, high voltage silicon detectors (L00 style)
  - ð To retain tracking capability we need at least twice as many detectors: ⇨ **More silicon**
  - ð To survive higher radiation dose we need to operate the silicon at a lower temperature
    - – **Sensors must be actively cooled**
- The current SVX3 chip (Honeywell 0.8um) cannot survive
  - ð The SVX4 chip is being designed. Uses naturally rad-hard 0.25um standard technology

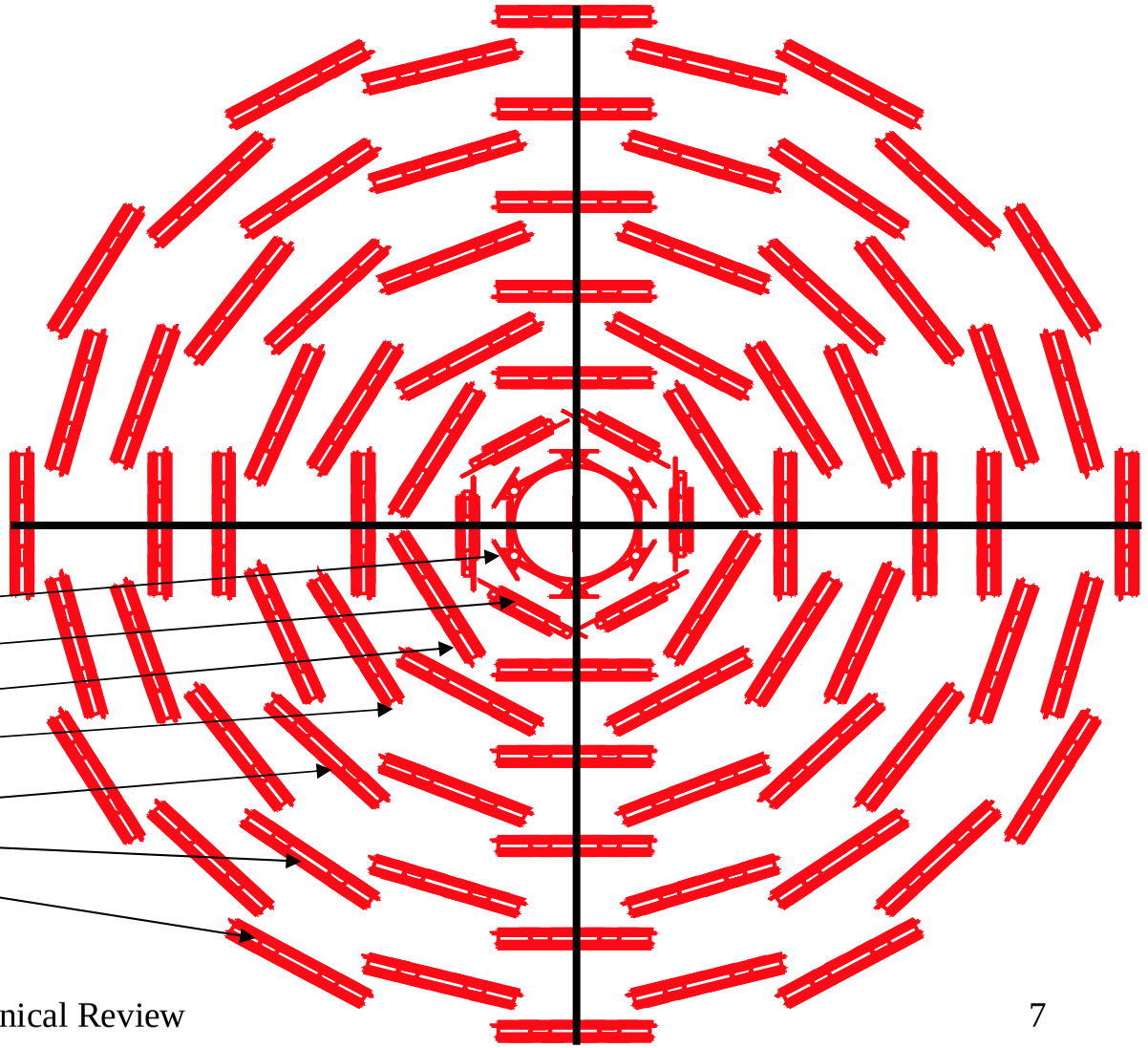


Silicon Upgrade for Run IIB

- **Goal: Ready for installation by Jan. 2005!**
- **Short turn around (~6m) between Run IIA and IIB**
  - ð Only viable option is complete replacement
- **Design Goals:**
  - ð Robust, simple and reliable design
  - ð Minimize the cost
  - ð Match or exceed performance of Run IIA silicon detector
  - ð Minimize changes to infrastructure: DAQ or cooling systems
- Pursue common solutions with D0 through task force meetings: chip, sensor specs, beampipe,…
- **Changed design since TDR in response to PAC recommendations: Dropped an inner layer!**

Run IIB TDR Layout

- Double sided staves: axial and stereo sensors
- Uniform design for L2-6
- 4-fold symmetry for L2-6)
- L1 very similar to L2-6
- L0 ~ L00 with only 2-chip sensors and supported by beam-pipe

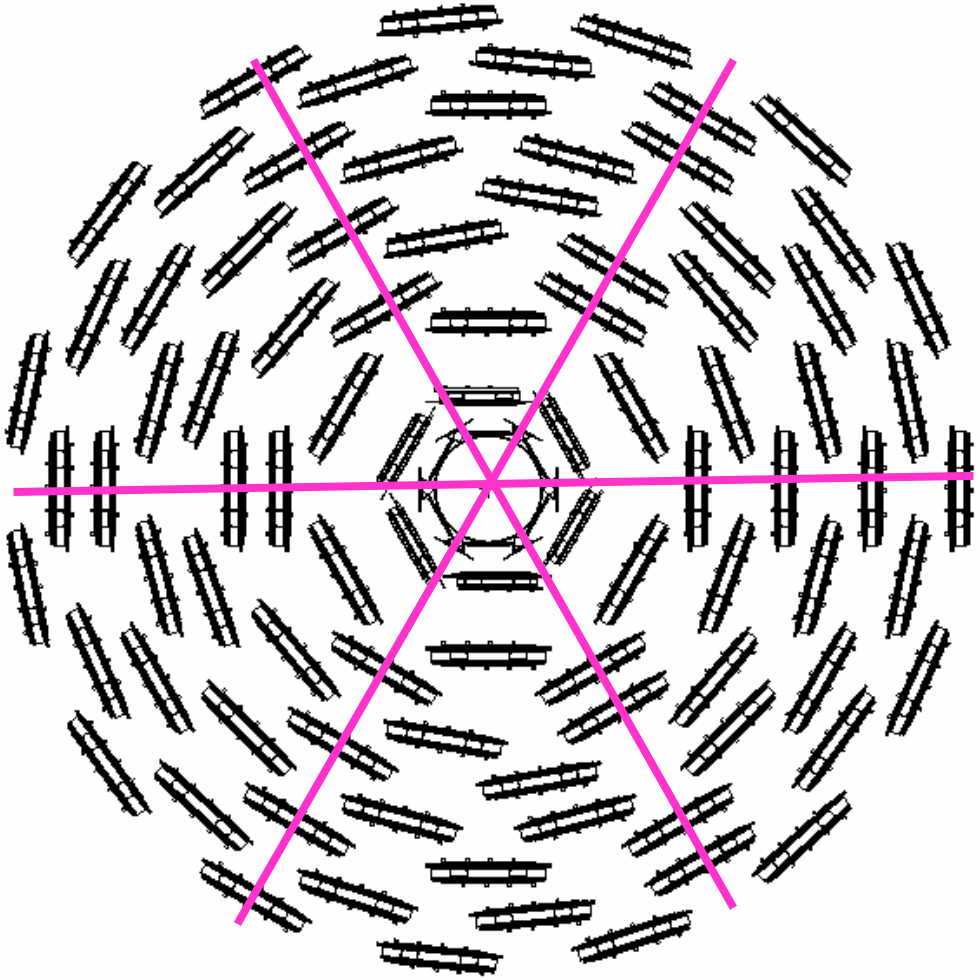


Layer 0: 12 fold Axial
Layer 1: 6 fold Axial-90
Layer 2: 6 fold Axial-90
Layer 3: 12 fold Axial-90
Layer 4: 16 fold Axial-2.5
Layer 5: 20 fold Axial-2.5
Layer 6:24 fold Axial -90

New 6-fold layout

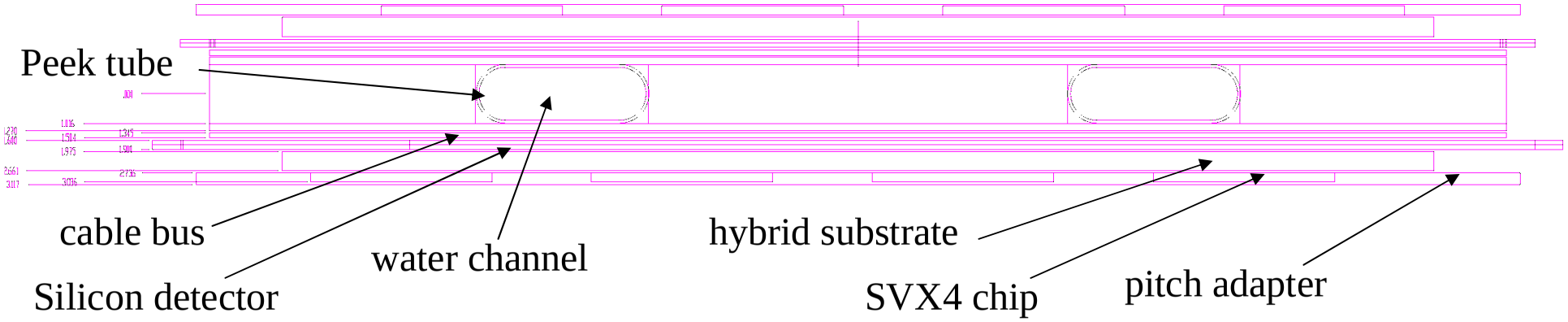
Changes from 4-fold design

- Dropped Layer 2!
- One outer layer stave design
- More symmetric
- Less overlaps
- Smaller pitch



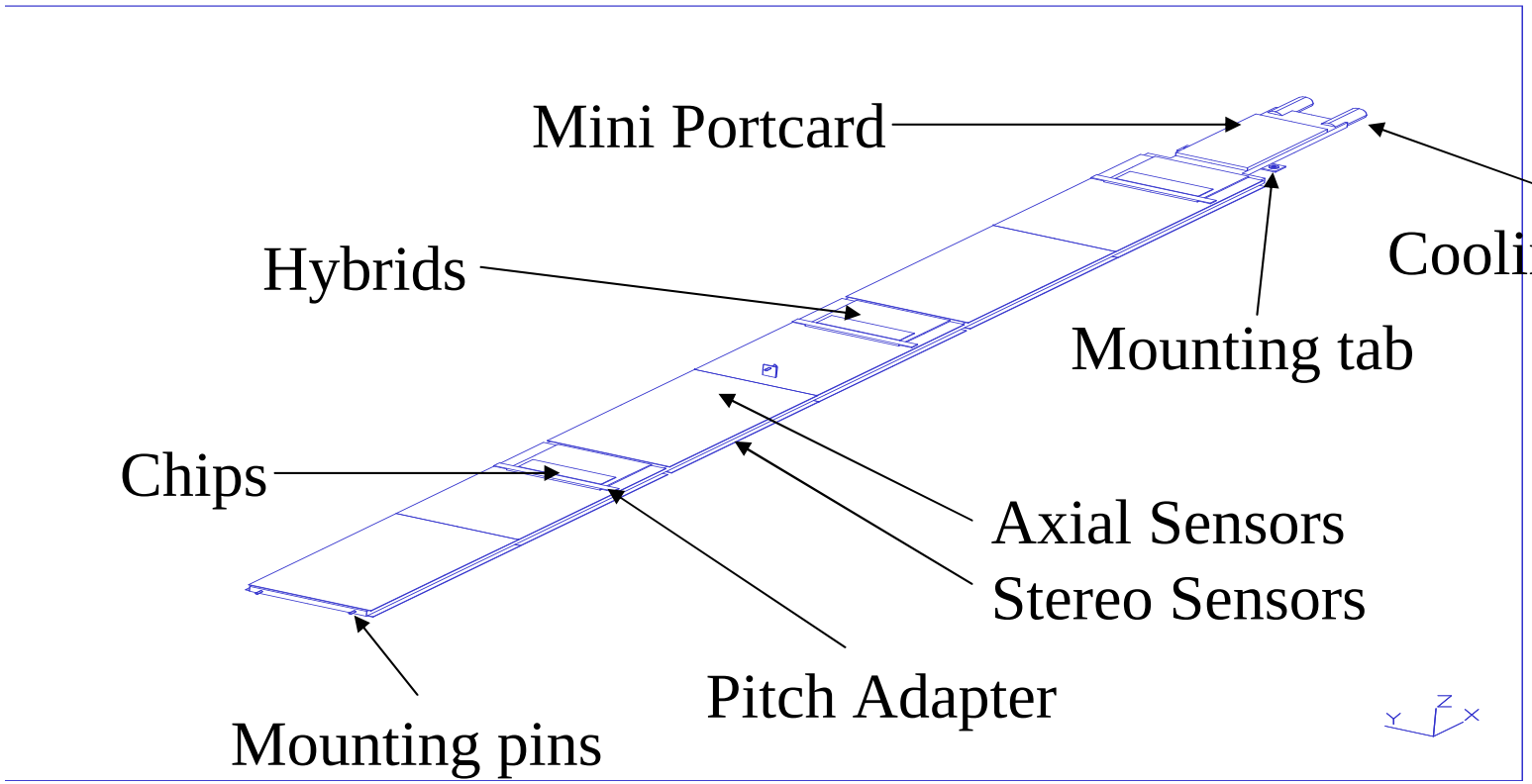
Layer 0: 12 fold Axial
Layer 1: 6 fold Axial-Stereo (90º)
Layer 2: 12 fold Axial-Stereo (90º)
Layer 3: 18 fold Axial-Stereo (2.5º)
Layer 4: 24 fold Axial-Stereo (2.5º)
Layer 5: 30 fold Axial–Stereo (90º)

Run IIB Staves



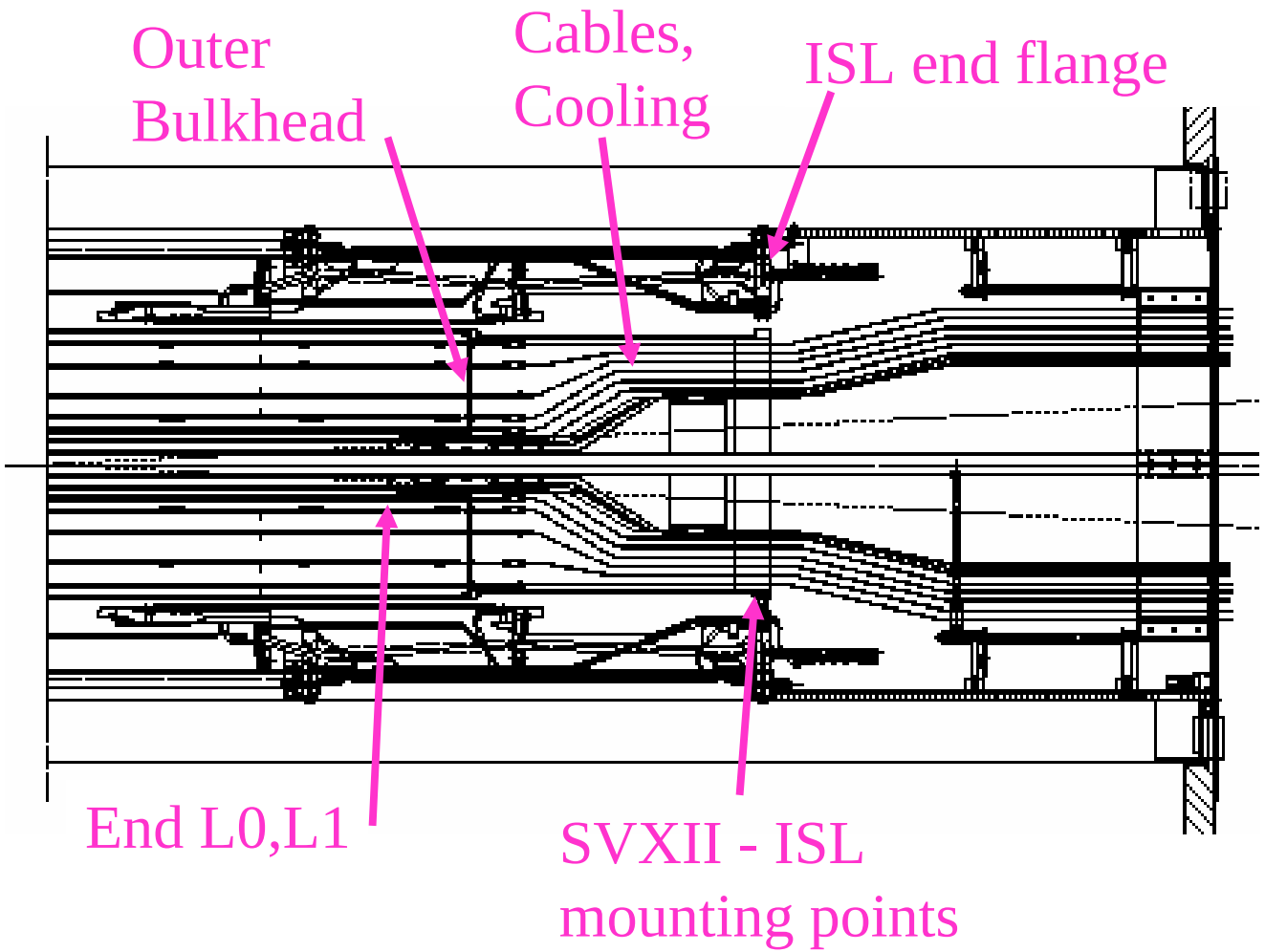
- Stave structure (60 cm long, supported at z=0 and +-60cm):
  - ð Carbon fiber – rohacell structure with ~2x6 mm peek cooling pipes
  - ð On each side:
    - 6 single sided silicon sensors
    - 3 hybrids glued to the silicon.
  - ð Silicon glued to copper-kapton bus cables
  - ð Hybrids wirebonded to bus cables through gaps between sensors
  - ð At end of stave a mini portcard with is bonded to the bus. It regenerates the signals to/from the SVX4 chips.

Run IIB Stave



Side View of Run IIB

- L0, L1 sensors
  - ð 74.7mm long
  - ð 93cm total
- L2-5 sensors
  - ð 97 mm long
  - ð 120cm total



Run IIB Layout Details

Layer	Fold	Type	Radius (mm.)	pitch/RO (um)	angle	Sensors	Hybrids	#chips
0	12	Axial	19.5 and 23.5	50/25	0	144	72	144
1	6	Stereo	30	95/47.5	90	72	36	144
1	6	Axial	33.5	60/30	0	72	36	144
2	12	Stereo	55 and 69.5	93/46.5	90	144	72	288
2	12	Axial	59.5 and 74	70/35	0	144	72	288
3	18	Stereo	85 and 99.5	80/40	2.5	216	108	432
3	18	Axial	89.5 and 104	70/35	0	216	108	432
4	24	Stereo	115 and 129.5	80/40	2.5	288	144	576
4	24	Axial	119.5 and 134	70/35	0	288	144	576
5	30	Stereo	145 and 159.5	93/46.5	90	360	180	720
5	30	Axial	149.5 and 164	70/35	0	360	180	720
				Totals		**2304**	**1152**	**4464**
				Totals SVXII + L00		**864**	**768**	**3276**
				Total Increase		**267%**	**150%**	**136%**

1008/1152 (88%) of hybrids are 4-chip

Run IIB Layout

- Uniform stave (ladder) design for ~90% of the detector
  - ð L2-5 = 168 staves - only one set of fixturing to develop

  (SVXIIA had 180 ladders, 5 different sizes, 36 of each size)
  - ð L1 = 12 staves – similar to L2-5
  - ð L0 ~ L00 type construction
- Small number of different parts
  - ð Only 3 types of hybrids (SVXII +L00 had 12 hybrid types)
  - ð L2-5 have 3 sensor types (SVXII had 5)
  - ð L1 has 2 sensor types (axial and stereo)
  - ð L0 has 1 type of sensors (L00 had 2 types)
- Construction flexibility
  - ð Stave design independent of sensor type (axial-90, axial-SA, or AA)
  - ð Decision needed before order of production sensors (Spring ‘02)
  - ð Replacing 90’s with axial or small angle would save ~250k$ in sensor costs
  - ð Can swap Layers 2-5 → Flexible additional descoping possible late in project

Run IIB Design Status

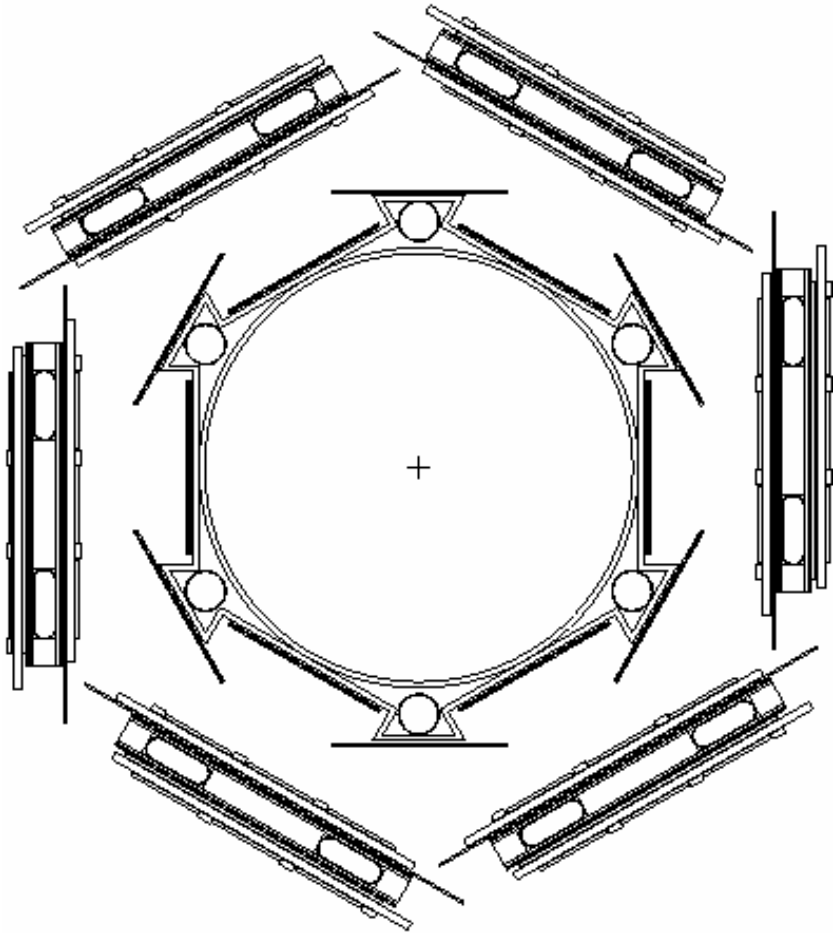
- L00 and Outer layers (2-5) design is fixed
  - ð Concentrate on outer layer prototyping
  - ð Outer layer sensor order is in progress
  - ð Hybrid and bus cable designs being finalized (Sign-off Dec. 13th, submit before Xmas)
- Layer 1
  - ð Most important layer for pointing into L0 (busiest)
  - ð Provides backup if Layer 0 hit is missed or confused
  - ð Smallest possible R
  - ð Complete coverage
  - ð Smallest possible pitch
  - ð Electronics from L0 and L1 constrain space
  - ð Currently a work-in-progress

Inner Layers Baseline

Design sensors and hybrids to fit

- Smallest radius
  - Ø Axial ~ 34mm
  - ØStereo ~ 30mm

- Small pitch (60/30um)



Inner Layer Descoped Option

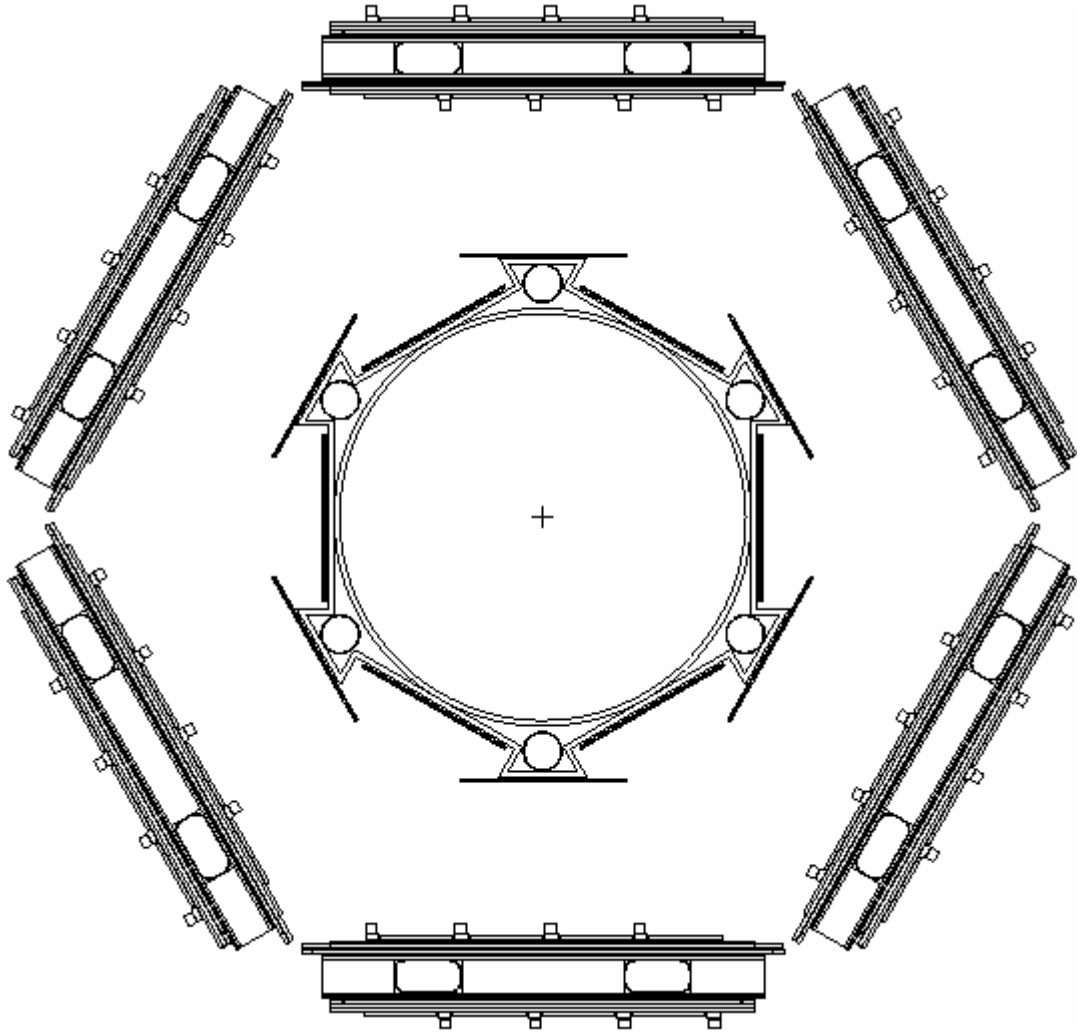
Use outer layer stave for Layer 1

Large stave limits options for radial placement

R Axial ~43mm vs 34mm

Incomplete coverage

But could save ~500k$

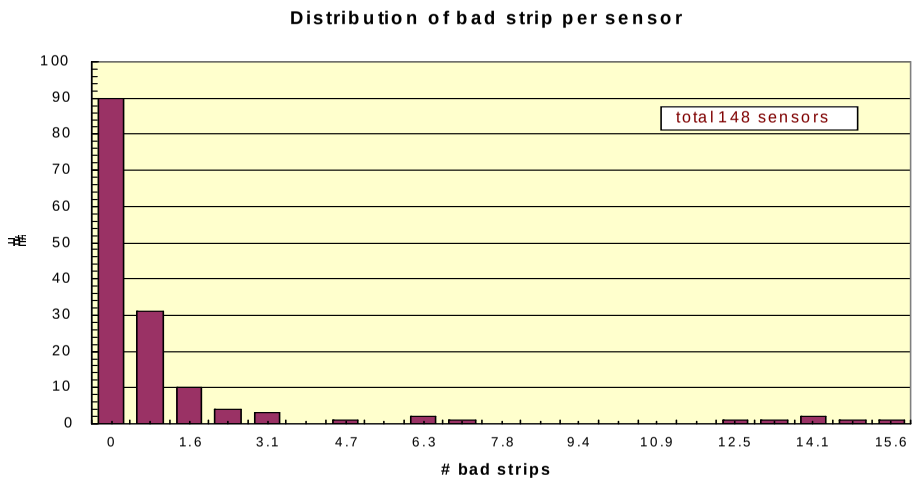


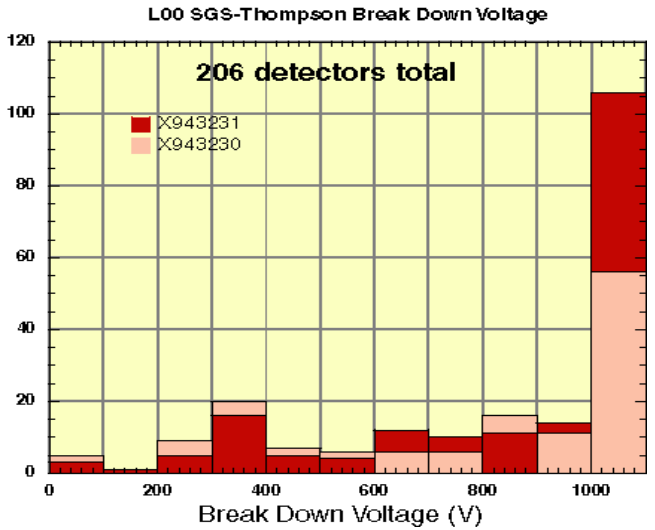
Layer 0 Design

- Inner Layer (L0) follows Run IIA L00 design
  - ð Fine pitch cables connect sensors to hybrids
  - ð Hybrids are located out of tracking volume
  - ð Hybrids ~identical to L00
  - ð Low mass construction is of utmost importance for 1st measurement
- Limit cost and risk in assembly process
  - ð Fine Pitch Signal Cables (L00 style) used only on L0
  - ð Having hybrids glued to silicon for majority of layers is great benefit in terms of ease of assembly, handling, testing, commissioning
  - ð Additional material/layer is small (0.3%X0) and effect of material is reduced for outer layers.
- Prototype efforts on cables are underway using L00 layout

Silicon Sensors

- All detectors are single sided and based on the high voltage operation layout (CMS,ATLAS,L00)
  - ð Easy to build, test and handle
  - ð Minimal R&D necessary
  - ð High yield and a minimum number of problematic channels is expected (<1% in most of the detectors)
  - ð Mask Designs nearing completion – prototype orders in progress
- Experience with L00 Sensors:





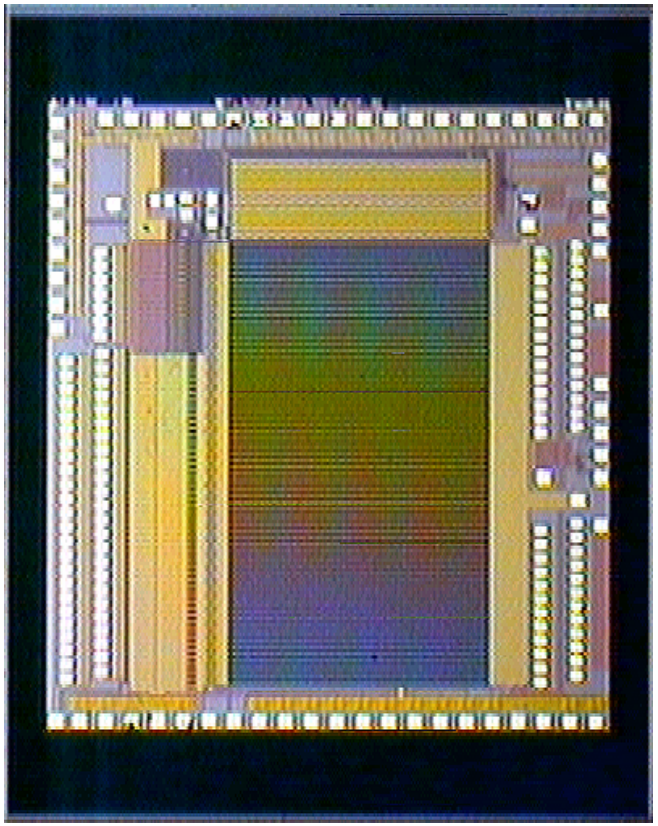
SVX4 Chip

Great progress since last PAC Meeting

- Test chips came back in early August – entire frontend (preamp + pipeline) functions!
- Chips irradiated to 16 Mrad with Co-60 facility, no changes observed –T.Zimmerman "If some of the other components on the board hadn't melted, I wouldn't have believed it was irradiated. ''
- S/N 30% better than SVX3
- CDF and D0 use same chip

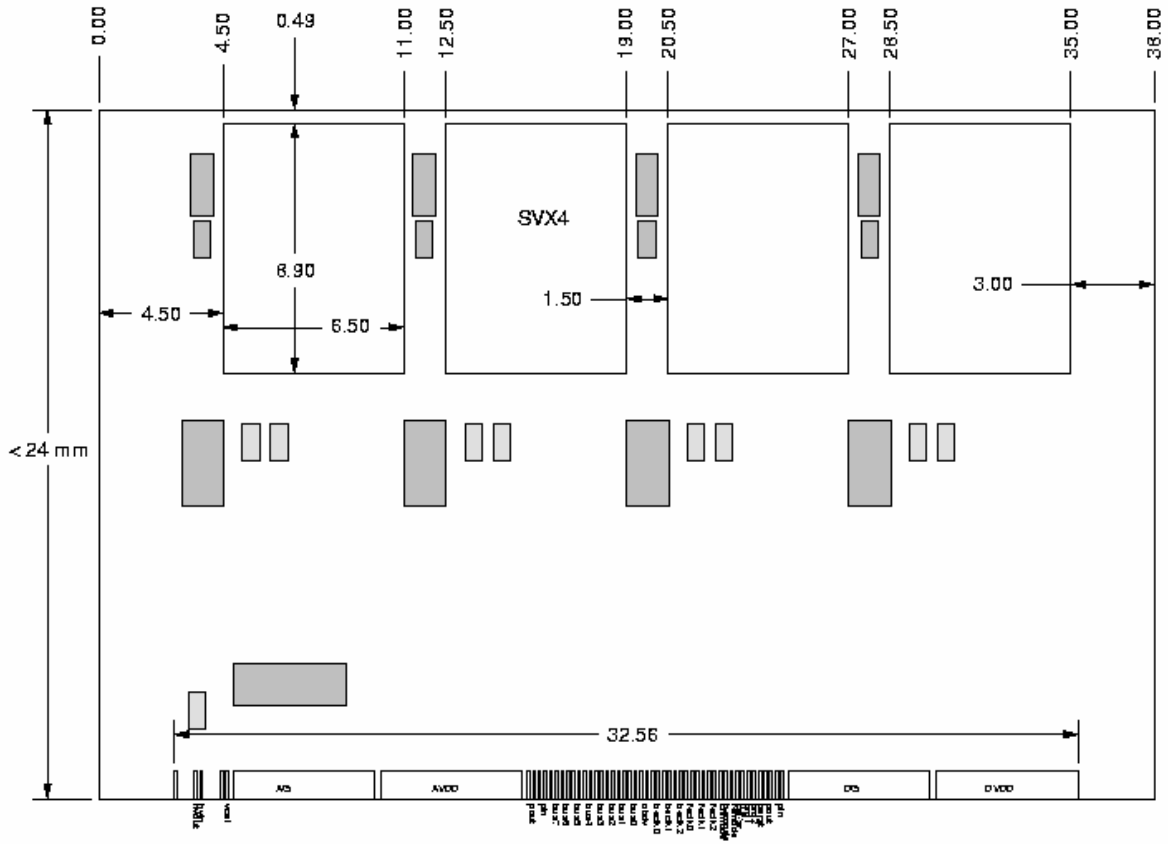
October 22 SVX4 chip review found project is in reasonably good shape

- Full chip submission expected Dec. 21st
- Will have chips by end Feb. (8 week turn-around)



Outer Layer Hybrid Layout

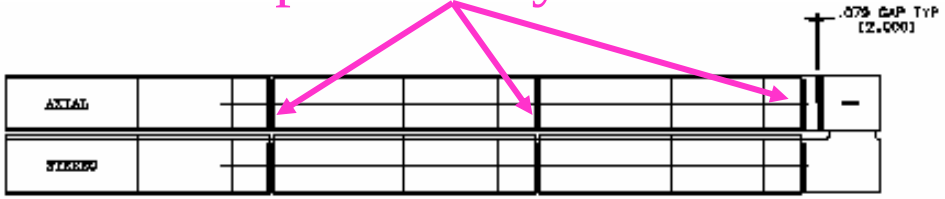
- New technology (used on L00) with 50µm trace/50µm space and 100µm via pitch
- Can now fit a power bus layer and signal traces on a single layer, reducing the total number of layers to 4
- Result is a much smaller hybrid wrt SVXII: 24x38mm



CDF Run2b Silicon 4 chip hybrid layout V3
11/29/2001

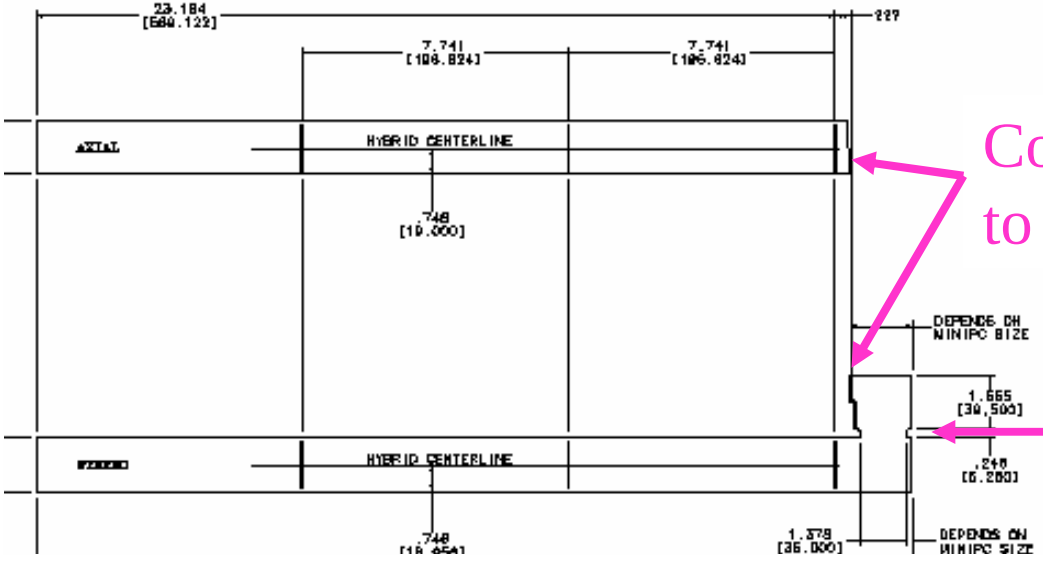
Bus Cable Profile

Bond pads for hybrids



Axial

Stereo



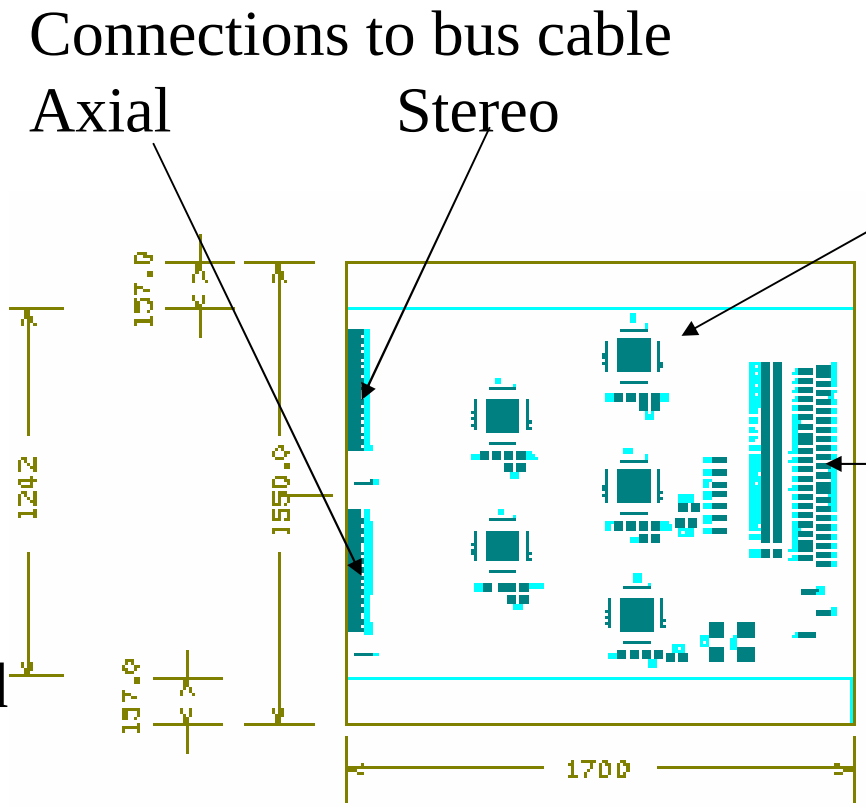
Connections to MPC

Cable Fold-over

Mini Portcard Layout

Use BeO for substrate (380um thick)

3 layers of traces
Plus power and ground

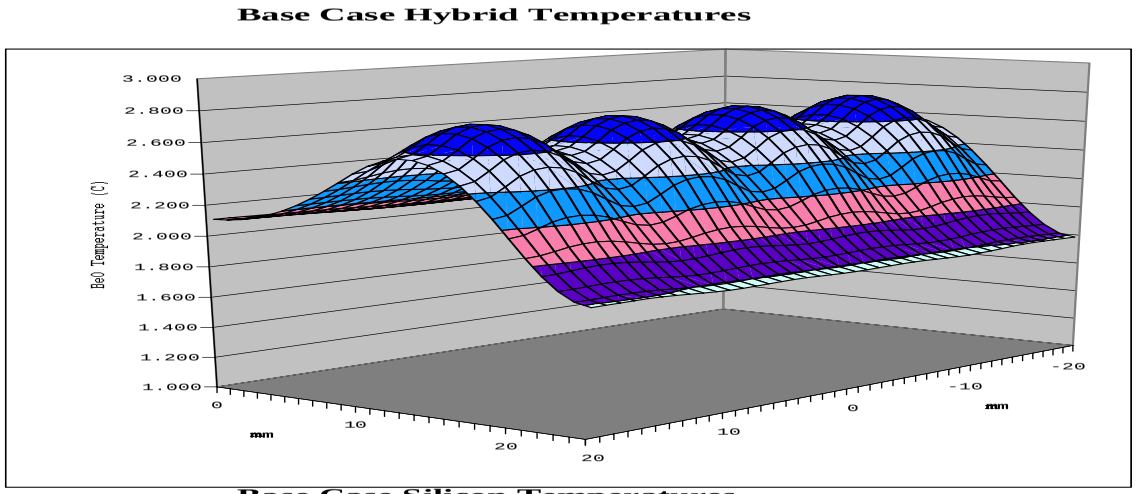


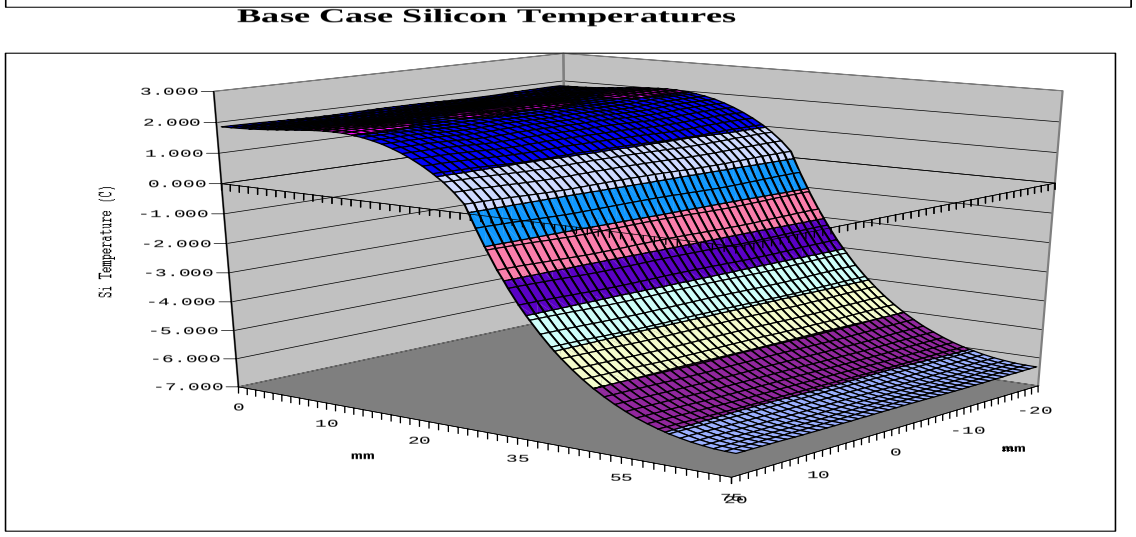
Radiation Damage and Cooling

- Keep silicon cool to limit the amount of noise increase due to leakage current and limit the reverse annealing effect
- Studies of these effects set temperature limits: for S/N >10 for 30 fb^{-1}
  - Layers 4-5: T<15^{o} C
  - Layers 2 and 3: T<10^{o} C
  - Layers 0 and 1: T<-5^{o} C
- Requires active cooling of staves
  - Cooling tubes integrated into stave structure
- Total heat load very similar to Run IIA ~3KW
- Can use existing cooling system with increased glycol concentration (43%) for operation at -20^{o}C

Cooling Studies

- Model:
  - ð 4-chips hybrid over one sensor
  - ð Hybrid is 15milBeO, 25mm long
  - ð Silicon is 0.3x75
  - ð Bus cable is 0.214 thick with 0.18W/m-K
  - ð Core skin is 3 plies Carbon fiber
  - ð Cooling tube is peek 0.1mm thick and 5mm flat area
  - ð Coolant T=-9C
  - ð Convection to10C gas



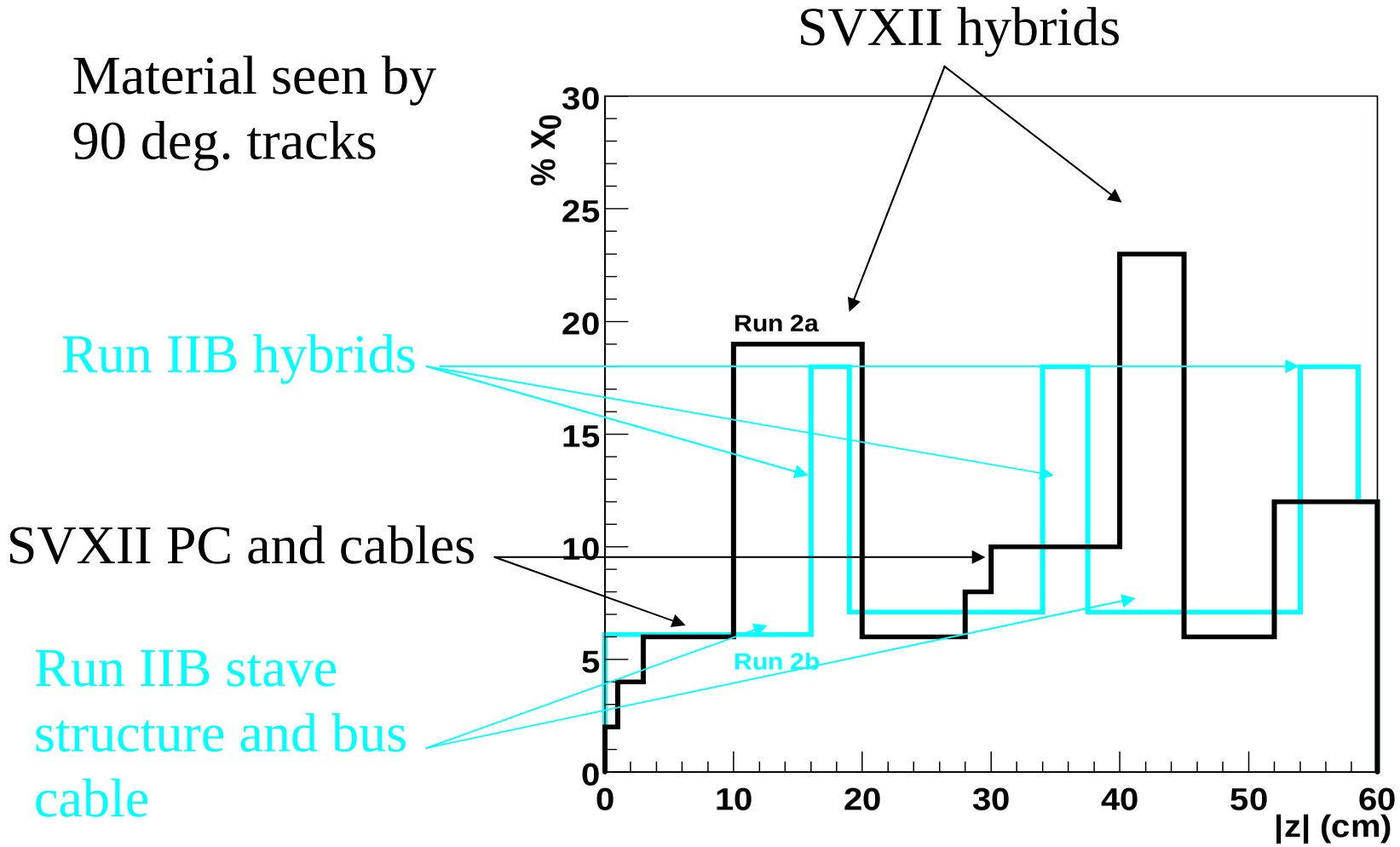


Stave Material and Stiffness

- Stiffness traded for light construction
- Average materials over area of stave: 1.5% X0 per stave:
  - ð 42% of total is in silicon sensors (2 sensors 320um thick =0.64X0)
  - ð 33% in CF, cooling tubes, water, glue
  - ð 12% in hybrids
  - ð 9% in bus cable
  - ð 4% in MiniPC (actually outside tracking region)
- Can tolerate ±80μm radial deviation from a plane over a module (~20cm)
- FEA of structure found that sag was ~170μm over 60 cm length
- Can reduce sag by increasing thickness of Rohacell foam with little change in mass
- No need for midspan support mentioned in TDR
- Making prototypes to verify FEA results – reasonable agreement

Compare Material in Run IIA with IIB

Material seen by
90 deg. tracks



DAQ Changes from Run IIA

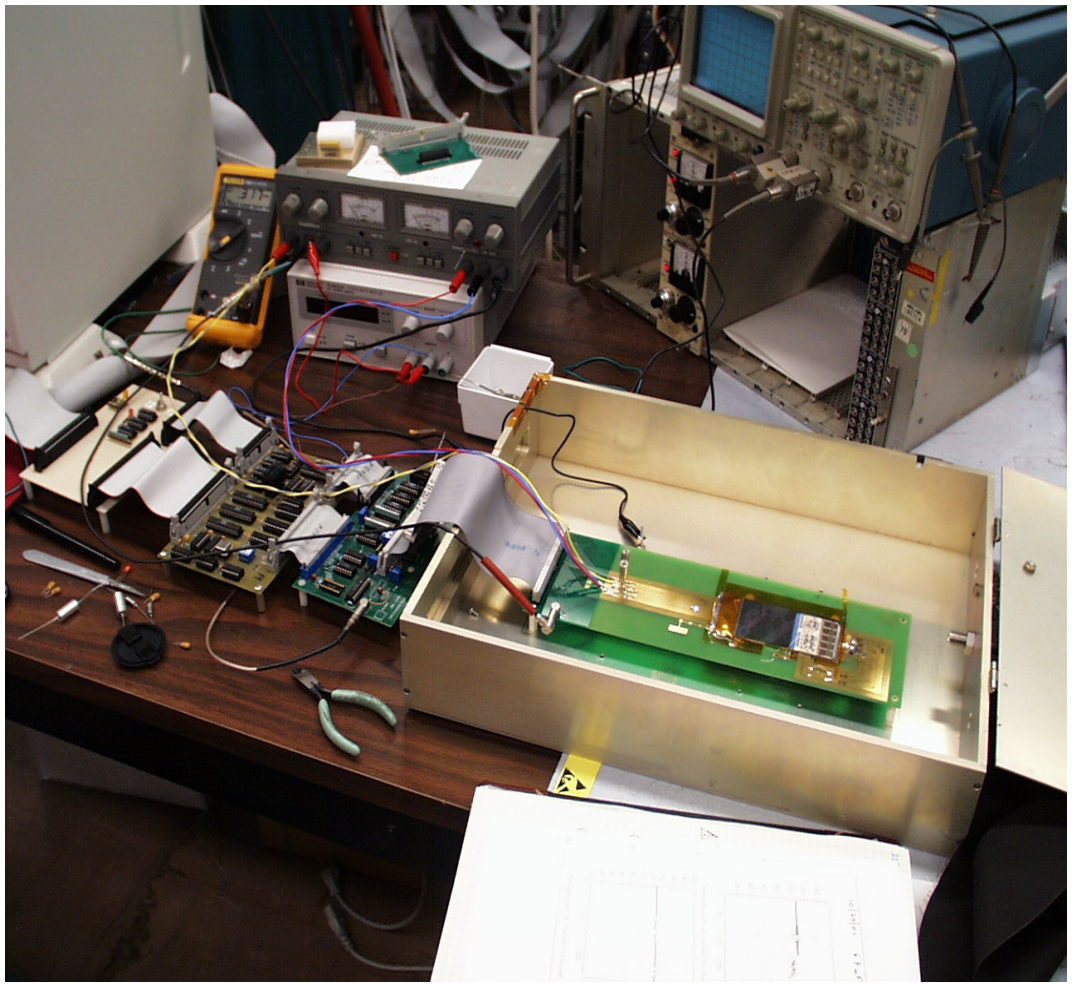
- New chip requires changes in front end of DAQ: New hybrids (smaller!)
- Optical components unavailable and not rad hard:
  - New mini portcards (smaller, minimal active components)
  - New Fiber Transition Modules (No Fibers!, use copper instead)
- New Power Supplies: off-the-shelf, not custom
- No changes upstream of the FTMs
- Reduced mass in tracking volume and improved accessibility
- Significant reduction in number of different components
- Number of readout chains fits in existing infrastructure
- SVT can be enhanced to work with Run IIB layout
  - Modifications similar to those already made for L00

Electrical Prototyping of Stave Bus

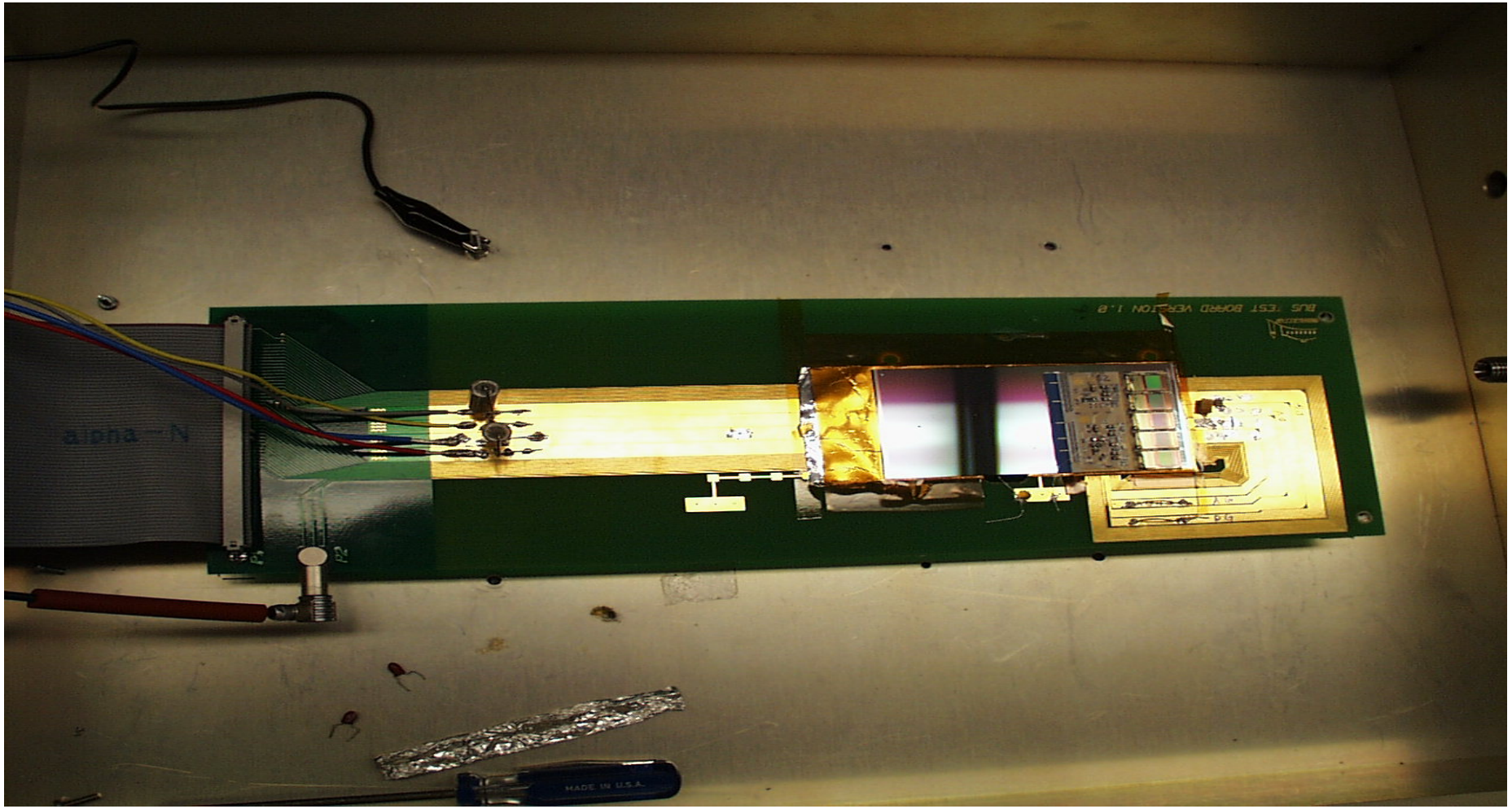
- Proposed stave concept uses a data, control, and power distribution bus which is placed underneath the silicon detectors.
  - ð Potential capacitive coupling of digital signals into the detector backplane and SVX4 front ends.
- Issue is particularly for deadtimeless operation
- Basic approach to control of coupling:
  - ð Shielding and insulation layer thickness
  - ð grounding and power distribution
  - ð pulse shapes, timing, and current
  - ð Challenge is to minimize coupling while maintaining low mass bus.
  - ð Bus prototype has been constructed and study is under-way

Electrical Bus Prototype tests

- Pre-prototype bus built into G10 board
- Use leftover SVX' layer 4 sensor (single sided) and SVXII hybrid
- Test setup at LBL used to study different configurations of grounding and shielding



Electrical Bus Prototype tests



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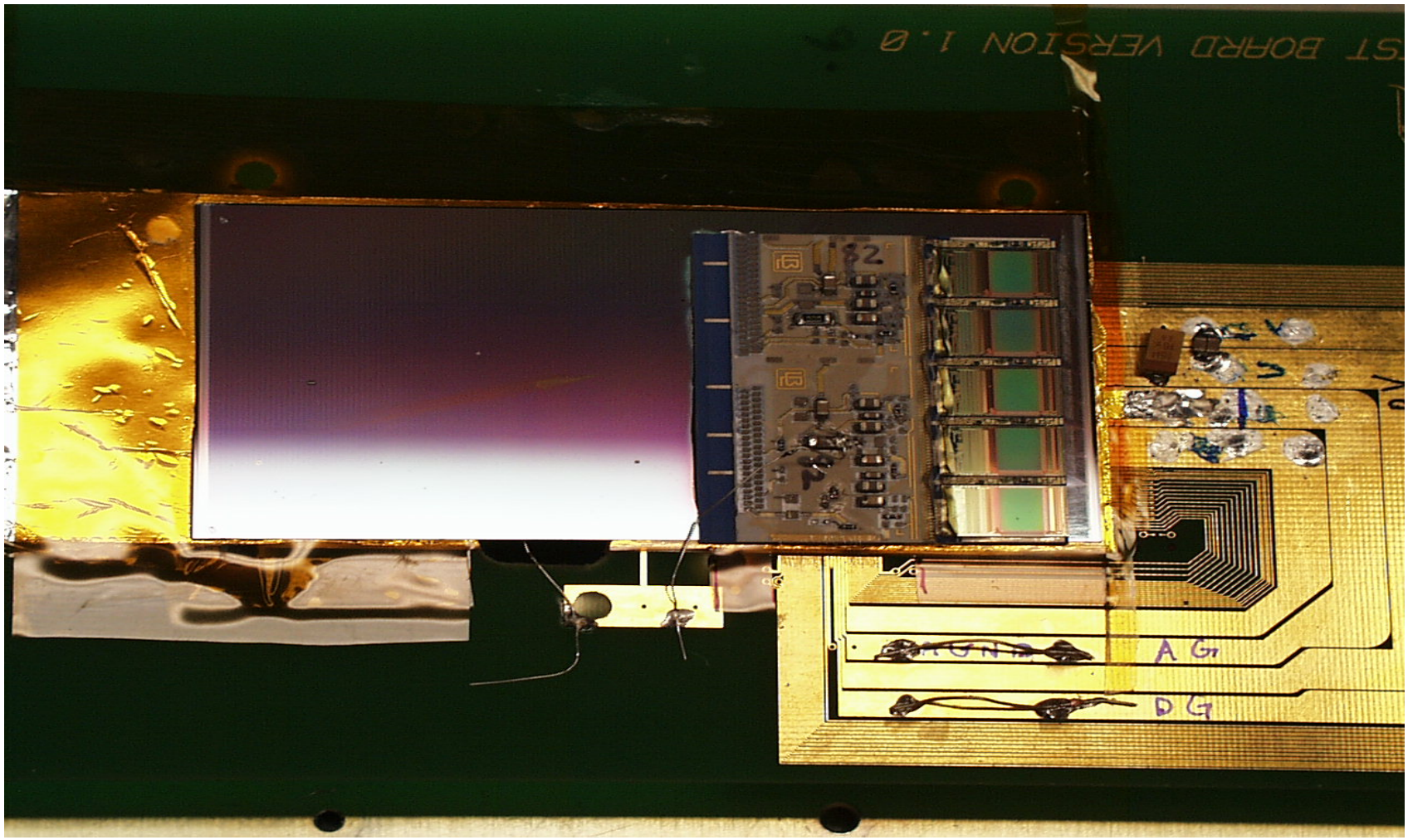


Prototype Stave Bus Findings:

- Without shield
  - ð clear coupling can be seen and spatially correlated with specific activity on bus (clocks, data buses, etc)
- With 10 micron Al foil (assumed in material estimates)
  - ð all spatial effects are erased. Some overall coupling remains.
- Pedestal shifts seen during mode transitions when power consumption changes can be reduced by grounding changes and bypassing.
- Further improvement expected from changes in grounding and signal conditioning. Present shield thickness is probably sufficient.

Tracking Studies – dropping layer 4 or 5

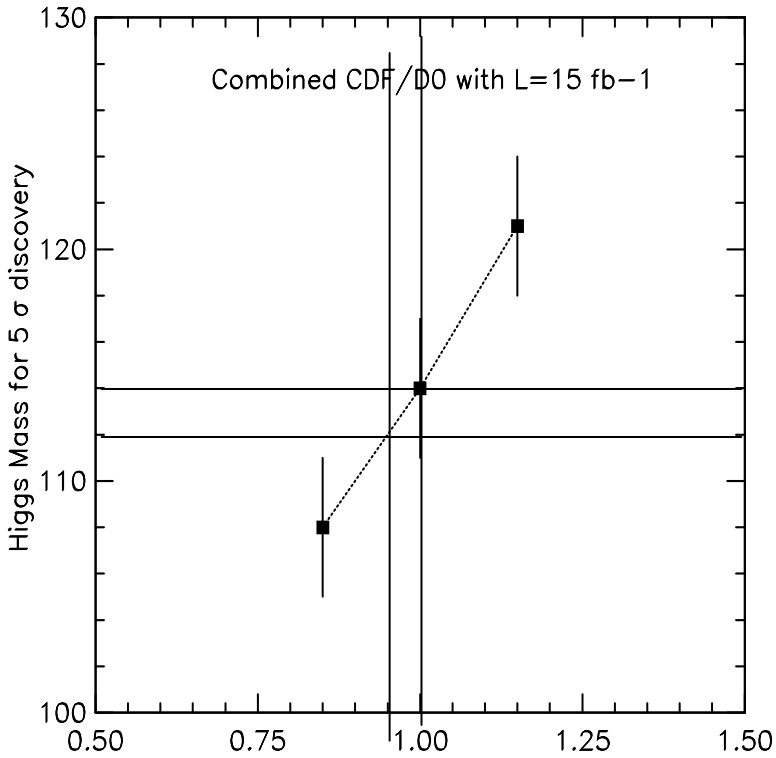
- Use Run 2A simulation (well studied), ISAJET MC and ttbar events.
- Study tracking (OI) and b-tagging efficiencies for different configurations
  - ð A: Baseline = Run 2a = L00 + 5 SVX layers + ISL and COT
  - ð B: Drop Layer 5 of SVXII
  - ð C: Inner axial and stereo layers of COT dead and drop L5
  - ð D: Inner COT layers dead and drop L4
- b-tag ≡ 3σ Lxy for a jet. Results for 1000 events, stat. unc.~1.3%
- Fake track ≡ (MC d0 – found d0)>3σ for a prompt track. 100 Evts,stat. unc. ~0.5%

	B-tag Eff. (%)	% Change
A	58.8	-
B	56.3	-4
C	51.3	-12.6
D	51.0	-13.3

	% Fake Tracks	% Change
A	7.7	-
B	8.9	+16%
C	9.5	+23%
D	8.7	+ 13%

Higgs discovery vs Btag eff.

- B tagging is critical for light Higgs discovery
- Higgs working group found direct relationship (significance$\propto$L*eff^2).
- For a 4% reduction in b-tag efficiency (CDF and D0)
  - ð ~ 3 GeV less mass reach
  - ð ~ 14% more luminosity is required



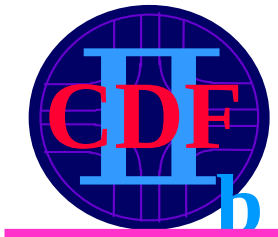
Relative b-tag efficiency
(1= 65%)

Effect of dropping layer 4 or 5

- Reduction in b tag eff. from dropping an outer layer could be compounded by degraded COT performance due to aging and/or high occupancies
- The quoted 4% reduction represents a minimum!
  - ð additional fakes (16%) would force tighter cuts and reduced efficiencies
  - ð Multiple interactions at high luminosity will become problematic
  - ð The effect will be greater for stand alone tracking (which is used for the forward region or ~30% of acceptance)
- Dropping layer 4 or 5 layer would require at least ~14% more luminosity, or would lower the discovery mass reach by >~3 GeV

Conclusions

- Highly modular and buildable design for the Run IIB Silicon Detector
- Maintains the tracking capability of the CDF detector
- Total mass in tracking volume is reduced
- DAQ simplified, active components are more accessible
- Design has been simplified since TDR by dropping a layer.
- Optimization of Layer 1 design is in progress
- Design and prototyping efforts are underway for outer layer components – hope to place orders before the holidays.
- Finding the Higgs will be difficult, we need as much b-tagging efficiency and redundancy as possible.



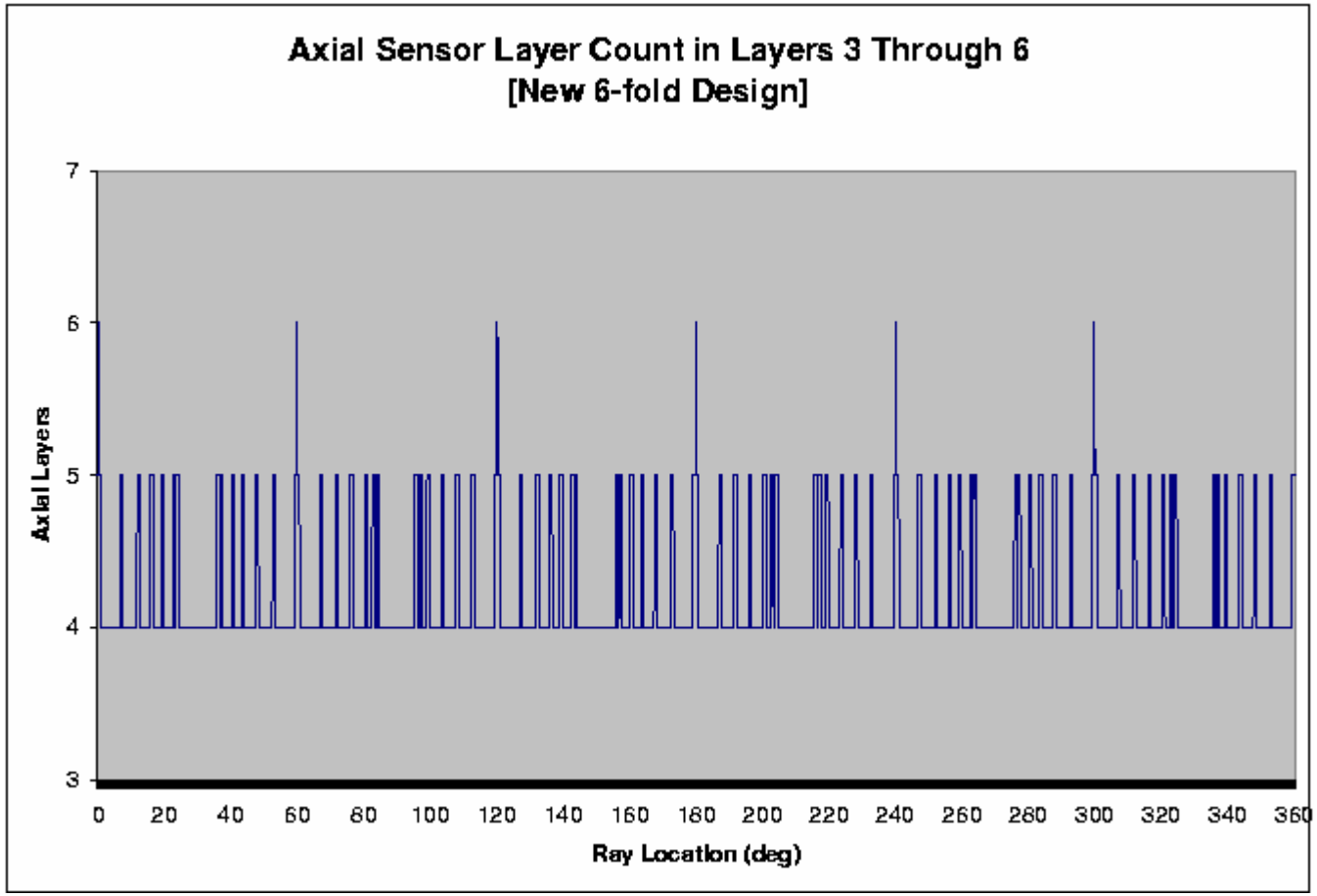
Stave Material

part name	material	X0	length	width	thick	num	factor	scale T	% X0	% of total	subtotal %	
detectors	silicon	93.6	92.5	47	0.32	12	1	0.596	0.637	42.335	42.335	
carbon fiber facin	CF	230	561	47	0.25	2	1	0.471	0.205	13.605		
foam	rohacell	13800	561	47	3	1	1	2.824	0.020	1.361		
stave expoxy	epoxy	186	561	47	0.075	2	1	0.141	0.076	5.047		
peek tubing	PEEK	319	561	12	0.1	2	1	0.048	0.015	1.002		
water coolant	water	360	561	12	1.3	2	1	0.625	0.174	11.540	32.555	i, stave, cool
hybrid substrate	BeO	144	25	40	0.381	6	1	0.082	0.057	3.768		
dielectric	glass	100	25	40	0.038	18	1	0.024	0.024	1.624		
shield plane	Au	3.35	25	40	0.008	6	0.47	0.001	0.024	1.598		
gold planes powe	Au	3.35	12	40	0.008	6	0.47	0.000	0.012	0.767		
gold planes grour	Au	3.35	12	40	0.008	6	0.47	0.000	0.012	0.767		
gold traces	Au	3.35	25	40	0.006	12	0.094	0.000	0.007	0.480		
SVX4 chips	silicon	93.6	10	6.8	0.3	24	1	0.017	0.019	1.242		
conducting epoxi	silver*	8.54	10	6.8	0.025	24	0.1	0.000	0.002	0.113		
ceramic caps 080	dielectric	35	2	1	1.2	12	1	0.001	0.003	0.195		
ceramic caps 120	dielectric	35	3.2	1.6	1.27	6	1	0.001	0.004	0.265		
ceramic caps 060	dielectric	35	1.6	0.8	0.9	48	1	0.002	0.006	0.375		
tantalum caps	tantalum	4	2	1.25	1	6	0.75	0.000	0.010	0.668		
resistors 0402	Al2O3	35	1	0.5	0.5	72	1	0.001	0.002	0.122	11.984	hybrids
bus kapton	kapton	287	440	40	0.025	4	1	0.063	0.022	1.456		
bus Cu traces	copper	14.3	440	32	0.017	2	0.81	0.014	0.097	6.436		
bus Al plane	aluminum	89	440	35	0.012	2	1	0.013	0.015	0.986	8.878	bus
fanout substrate	Al2O3	75.5	2.75	47	0.375	8	1	0.014	0.018	1.219		
fanout traces	aluminum	89	2.75	47	0.005	8	0.4	0.000	0.000	0.006		
MiniPC substrate	BeO	144	35	40	0.381	1	1	0.019	0.013	0.879		
dielectric	glass	100	25	40	0.038	8	1	0.011	0.011	0.722		
gold planes powe	Au	3.35	25	40	0.008	1	0.47	0.000	0.004	0.266		
gold planes grour	Au	3.35	25	40	0.008	1	0.47	0.000	0.004	0.266		
gold traces	Au	3.35	25	40	0.006	3	0.2	0.000	0.004	0.255		
XCVR chips	silicon	93.6	2	2	0.5	10	1	0.001	0.001	0.051		
conducting epoxi	silver*	8.54	2	2	0.025	10	0.1	0.000	0.000	0.003		
ceramic caps 080	dielectric	35	2	1	1.2	20	1	0.002	0.005	0.326		
tantalum caps	tantalum	4	2	1.25	1	2	0.75	0.000	0.003	0.223		
resistors 0402	Al2O3	35	1	0.5	0.5	20	1	0.000	0.001	0.034	4.249	mini-PC
	total								**1.504**			

Number of possible hits in L2-5 vs phi

6 hits – 0.2%

5-hits – 20%

4-hits – 80%

4 fold design:
6 hits – 5%
5 hits – 38%
4 hits – 58%