

# CDF Run II Silicon Tracking Projects<sup>\*</sup>

Alan Sill

*Department of Physics, Texas Tech University, Lubbock, TX 79409-1051, USA<sup>1</sup>*

for the CDF collaboration

---

## **Abstract**

Design features, functionality, and expected performance are reviewed for the silicon charged particle track detectors to be used by

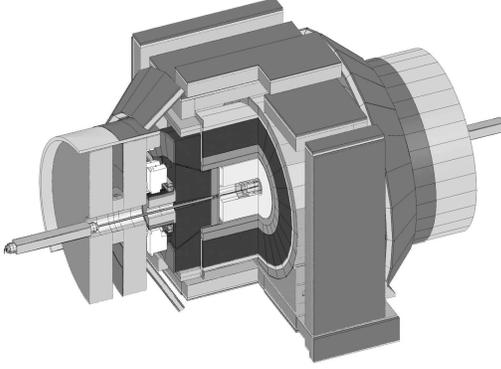


Fig. 1. An overview of the Collider Detector at Fermilab in its Run II configuration.

were distributed approximately as a gaussian along the beam ( $z$ ) direction, with an average standard deviation of typically 30 cm. The relatively short length of the silicon sensors limited the geometric acceptance to about 60% for single tracks[3,5], averaged over the luminous region. The angular acceptance for tracks from any given interaction was also limited by the previous geometry. Although detection of some tracks in forward and backward directions was possible for interactions that were displaced along the  $z$  direction from the center of the detector[4], more complete geometric coverage of the interaction region was clearly desirable.

For the next operating period of the accelerator, to be known as collider Run II, the expected instantaneous luminosity will be approximately an order of magnitude larger than the nominal values of up to  $2 \times 10^{31} \text{cm}^{-2} \text{s}^{-1}$  encountered during Run I. Changes planned for the CDF detector during Run II to meet this challenge include simplification and improvement of the angular range of

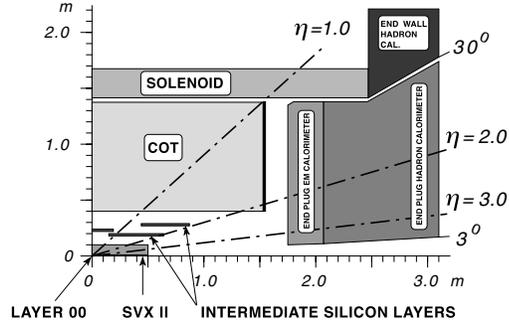


Fig. 2. A cutaway view of one quadrant of the inner portion of the CDF II detector showing the tracking region surrounded by the solenoid and endcap calorimeters.

the calorimetry and muon coverage, improvement of the speed of the electronics and trigger system, addition of a time of flight counter, and complete replacement of the charged particle track detectors, including the silicon detectors[5]. Figure 1 shows an isometric cutaway view of the planned configuration of the experiment once these changes are made.

Operation of the earlier Run I detectors, called SVX for the period between 1992 and 1993 and SVX' for the period between 1994 and early 1996, provided CDF with substantial experience in the electronics needs for readout[6] and radiation environment[7] to be expected in Tevatron hadron collisions. Detectors and electronics that can withstand several megarads of integrated dose are required to survive the radiation fields created by the higher Run II luminosity[5]. The beam crossing interval will be reduced by up to a factor of 25 to as little as 132 ns between bunches in order to reduce number of interactions per beam crossing. To avoid losing physics signals, elec-

tronics that can operate without downtime losses are preferred.

Goals to be achieved by this upgrade include the determination of precise 3-dimensional track impact parameters over as wide an acceptance range as possible to provide  $b$ -tagging for studies of top production, supersymmetry searches and the search for the Higgs boson. This detector and the associated trigger upgrades[8] will also be of great benefit to the CDF  $B$  physics program. Other goals for the Run II silicon system for CDF are to improve stereo tracking, to bridge more seamlessly between the vertex detector and outer tracker than in Run I, to improve the purity and efficiency of the tracking, and to increase the angular acceptance for well-reconstructed tracks [5,9].

## 2 Overview of the CDF Run II Silicon Design

To meet these goals, a central vertexing portion of the detector called the SVX II was designed, consisting of double-sided silicon sensors with a combination of both 90-degree and small-angle stereo layers[5,10]. The SVX II is nearly twice as long as the original SVX and SVX', which were constrained to fit within a previous gas-based track detector used to locate the position of interactions along the beam line. Further studies showed that this functionality could be provided by the SVX II itself, so the gas-based vertex detector was removed from the design and replaced by an additional set of silicon detec-

tors called the Intermediate Silicon Layers (ISL)[5,11].

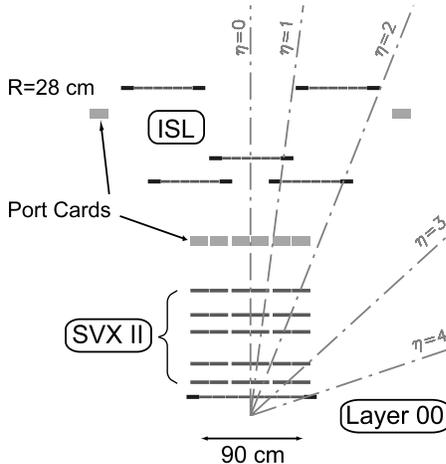


Fig. 3. A side view of half of the CDF Run II silicon system on a scale in which the  $z$  coordinate is highly compressed.

Due to readout speed and capacitance limitations that were most severe for the stereo layers, the readout electronics for the SVX II were designed to be mounted as close as possible to the sensors. The large instrumented length of silicon along the beam pipe requires these electronics to be located within the active sensitive volume, with resulting negative consequences on impact parameter resolution. To mitigate these effects, a layer of silicon called Layer 00 was added to the design at very small radius[9]. For capacitance and space reasons, to minimize material, and to allow large bias voltages to be used to ensure depletion even after extensive radiation damage, this layer is single-sided. The combined Layer 00+SVX II+ISL final design shown in Figure 2 functions as an integrated silicon tracker that recovers excellent  $r\phi$  impact parameter resolution without unduly affecting the  $z$  resolution of the experiment.

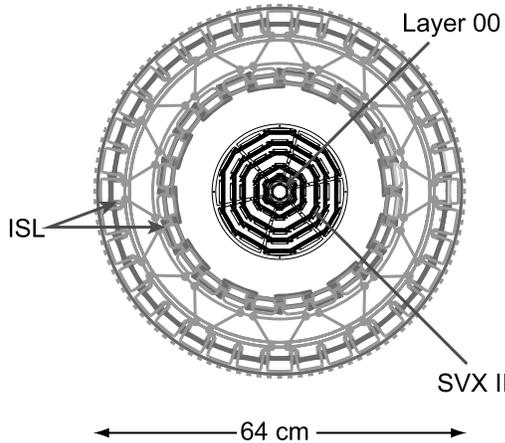


Fig. 4. An end view of the CDF II silicon system including the SVX II cooling bulkheads and ISL support structure.

A schematic view of the principal active components of the CDF Run II silicon system is given in Figures 3 and 4. The side view shown in Figure 3 is a cross-section of one half of the silicon tracker, using a compressed  $z$  scale. Figure 4 shows an end view of the CDF II silicon system including the SVX II bulkheads and ISL support frame. The total amount of material in the silicon system averaged over azimuthal angle and  $z$  varies roughly as 10% of a radiation length divided by the sine of the polar angle in the region of pseudorapidity  $\eta$  between 0 and 1. The average material traversed by particles increases to roughly twice this value for  $1 \leq \eta \leq 2$  due to the increased likelihood to encounter cables, cooling bulkheads, and portions of the support frame.

### 3 The SVX3D Readout Chip

All components of the CDF II silicon system achieve their data readout

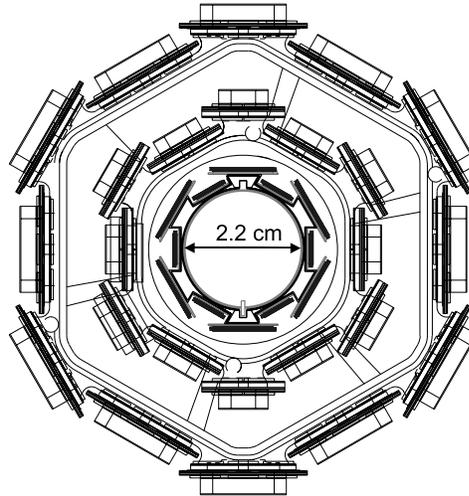


Fig. 5. End view of the innermost three layers of the CDF Run II silicon system, showing Layer 00 along with the first two layers of the SVX II region. The Layer 00 electronics (not shown) are mounted beyond the active volume for vertexing. The SVX II electronics are shown just outside and just inside of each of the layers drawn.

through a set of 128-channel custom integrated circuit chips with the designation SVX3. The design of this chip is currently at revision D, and includes preamplification, a multi-cell analog storage pipeline, and simultaneous analog and digital operation capability. An optional data acquisition mode allows common-mode noise to be reduced independently for each chip by dynamic data-driven determination of pedestal levels.

The physical layout of the SVX3D die is shown in Figure 6. The chip has been manufactured in both rad-soft and 0.8- $\mu\text{m}$  radiation hard CMOS processes, and in the latter version has been tested to operate successfully up to radiation doses of approximately 4 megarads[12].

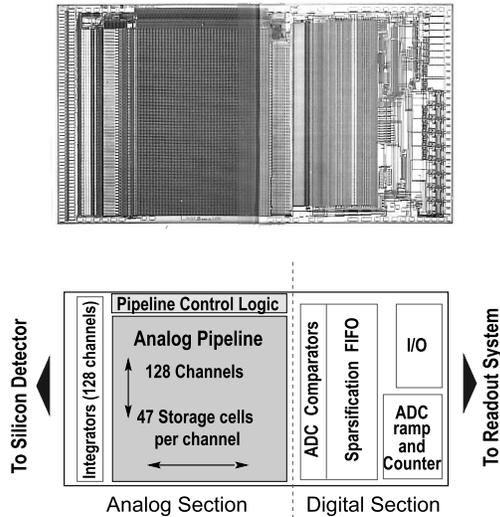


Fig. 6. A photo of the SVX3D readout chip is shown on the top. An organizational block diagram of its circuitry is given below. The analog and digital sections of the chip share a single die, with acceptably low crosstalk and noise.

Each channel of the SVX3D chip contains of a set of charge integrators followed by 47 cells of analog storage, and a Wilkenson analog-to-digital converter with 8 bits of precision, 7 of which are used. Readout in the back end of the digital section of the chip proceeds synchronously to a common bus and is controlled through serial instructions sent via multi-purpose mode and control lines. Sparsification, either with or without nearest-neighbor logic, is also provided and can be used whether or not the optional dynamic pedestal determination and subtraction mode is selected. The equivalent noise charge is roughly  $500 \text{ electrons} + 21 \text{ electrons per picofarad}$  at minimum bandwidth, rising to  $750 \text{ e} + 53 \text{ e/pF}$  at maximum bandwidth. Gain is selectable through an external resistor in the range between 300 and 4000 electrons per ADC count.

The chip is designed to operate at clock intervals between 100 and 400 ns, and takes approximately  $1.2 \mu\text{s}$  to digitize 7 bits of readout data. Each chip dissipates approximately 500 mW of power and is 11.9 by 6.3 millimeters in dimension. The chips are mounted onto multi-layer thick film ceramic hybrids to form multi-chip modules that serve as the basic units of readout in the data acquisition system. Single sided hybrids made of  $500 \mu\text{m}$  thick beryllia ( $\text{BeO}_2$ ) are used for the SVX II. The ISL hybrids are made from aluminum nitride and have chips mounted on both sides of the substrates. Layer 00 hybrids will most likely be made of alumina ( $\text{Al}_2\text{O}_3$ ) and be single-sided.

#### 4 Silicon Sensors and Ladders

The three main components of the silicon tracker each use different silicon sensor designs and layouts. Because it will be mounted closest to the beam, Layer 00 will consist of single-sided AC coupled p-in-n silicon with a guard structure designed to minimize leakage currents. This configuration is intended to improve radiation resistance[9]. Two widths of sensors (8.4 mm and 14.6 mm) will be interleaved in a 12-sided pattern that is physically mounted on and supported by the beam pipe. Each sensor will have a mechanical length of 78.4 mm and will be bonded to one other sensor to form pairs that are electrically 15.7 cm in active length. These sensors have an implant pitch of  $25 \mu\text{m}$ , implant

widths of  $8\ \mu\text{m}$ , and a readout pitch of  $50\ \mu\text{m}$  achieved by reading out alternate strips. Fine-pitch kapton cables carry signals from each of the six pairs of Layer 00 sensors to hybrids mounted at the ends of the array.

The next five layers of the tracker, which comprise the SVX II portion of the design, consist of wire-bonded pairs of double-sided detectors with readout electronics in the form of hybrids that are mounted directly to the silicon surface at each end of each four-sensor mechanical ladder assembly. The length of each ladder is 29 cm, with each consisting electrically of two half-ladders that are read out independently. A perspective view of one end of one of these assemblies is shown in Figure 7.

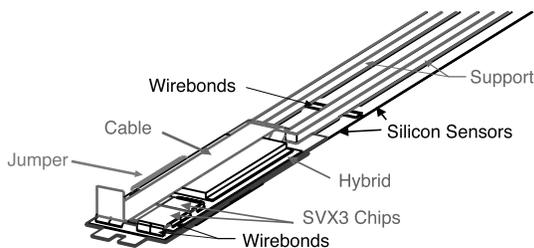


Fig. 7. One end of a 2-chip-wide version of the SVX II ladder.

Both 90-degree and small-angle stereo sensors are used in the SVX II, in the pattern  $(90, 90, -1.2, 90, +1.2)$  degrees for the n-strips from the innermost to outermost SVX II layers. All SVX II sensors are AC coupled,  $300\ \mu\text{m}$  thick, and biased using polysilicon resistors. The p-strips on the non-stereo side run in the axial direction of the detector and are used to measure the azimuthal angle  $\phi$  in the experiment. These strips are spaced in  $r\phi$  by approximately 60 to 65 microns, depending

on layer, and have implant widths of 14 to 15 microns. The stereo n-strips of the SVX II are spaced by  $(141, 125.5, 60, 141, 65)$  microns, and have implant widths of 20 microns for the  $90^\circ$  strips and 15 microns for the small-angle stereo layers. The  $90^\circ$  layers have an additional layer of insulator and readout strips in the “double-metal” configuration[14]; these strips carry the  $z$  signals to the SVX3 chips with a pitch that ranges from 58 to 60 microns depending on layer. The  $90^\circ$ -stereo sensors are manufactured by Hamamatsu Photonics. The small-angle stereo SVX II sensors are manufactured by Micron Semiconductor.

Common p-stops with widths of  $21\ \mu\text{m}$  along with individual p-stops of width  $15\ \mu\text{m}$  are used in the  $90^\circ$ -stereo layers. In the small-angle stereo SVX II layers, individual p-stops are not used, and the common p-stops have widths of 28 to 30 microns. Type inversion at high radiation doses might render these p-stops ineffective, but the n+ implants will remain isolated. Other radiation-induced effects will in practice limit the operating life of the sensors, such as the increased voltage necessary to achieve depletion, the resulting increases in current and dissipated power, and degradation of interstrip resistance with radiation[13].

Present estimates indicate that the innermost SVX II sensors will degrade beyond usable levels after the first 2 to 3 years of operation, corresponding to several  $\times 10^{13}\ \text{n/cm}^2$ [13]. Layer 00, which is single-sided and thus can operate acceptably even

when not fully depleted, should be able to withstand the higher radiation doses that it will encounter at its small inner radius. Along with the remaining layers of the SVX II and ISL, this should preserve functional  $r\phi$  tracking and at least some stereo capability to as much as  $5 \text{ fb}^{-1}$  of accumulated Tevatron data[9].

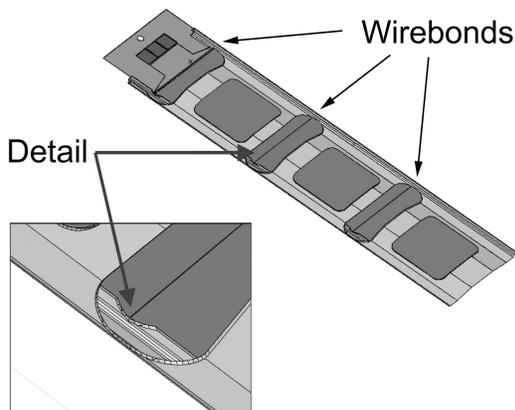


Fig. 8. A perspective view of the ISL ladder design.

The ISL portion of the tracker utilizes larger-pitch double sided sensors made in both 4" (Hamamatsu) and 6" (Micron) technology[15]. These sensors are also AC coupled, with polysilicon biasing and common p stops. A fixed strip pitch of  $112 \mu\text{m}$  is used on both the axial and 1.2-degree stereo sides. Pitch adapters are used to bring the signals from the strips to the more closely spaced inputs of the SVX3D chips. The stereo strips are on the n side for the Micron sensors and on the p side for the Hamamatsu sensors.

The ISL ladders are composed of six sensors, arranged as half-ladders of three sensors each. This arrangement is shown in Figure 8. Because of the larger strip pitch, positioning

tolerances for placement of these ladders are easier to achieve in the ISL. Taking advantage of the increased amount of space compared to the SVX II, these ladders overlap each other in  $z$  and are read out at each ladder end with double-sided hybrids that extend beyond the silicon. The innovative design of the carbon-fiber ladder support allows wirebonding to be done after the ladder has been assembled. This arrangement simplifies ladder construction and permits microbonds to be repaired even after assembly.

## 5 Structural and Cooling Considerations

The ISL space frame, shown in Figure 9, also supports the SVX II and all associated readout and utility components. (Layer 00 is supported by the beam pipe.) The central barrel of the ISL consists of silicon ladders that are staggered alternately at either 22.6 or 23.1 cm in radius from the nominal beam line. This layer is extended by an additional set of ladders mounted at 19.7 or 20.2 cm in radius that are contained in the barrels at each end of the space frame.

The outermost layer of the ISL is populated only in these end barrels, and consists of ladders mounted alternately at radii of either 28.6 or 29.0 cm. Temperature control is provided for the ISL electronics by a water/ethylene glycol coolant mixture flowing in aluminum tubes attached to beryllium ledges mounted on the space frame.

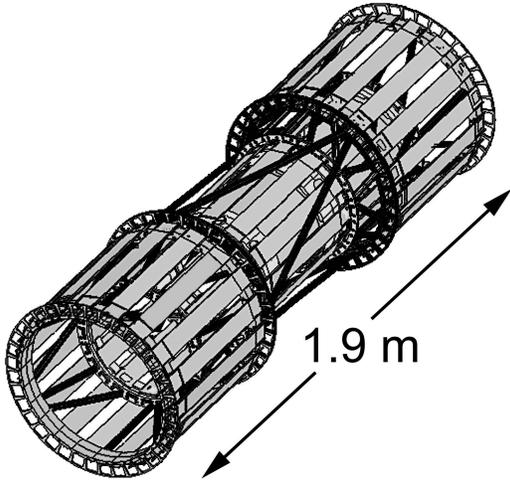


Fig. 9. A perspective view of the ISL space frame and silicon placement. For clarity, only every other silicon ladder assembly is shown.

The six layers of ladders that comprise the SVX II and Layer 00 portion of the tracker are arranged in twelve azimuthal wedges that alternate in radius within each layer. The SVX II sensors are arranged in three barrels, each four sensors in length. Water/glycol coolant for the silicon and electronics flows within internal channels that are machined into the beryllium bulkheads at each barrel end. The expected silicon temperature in the SVX II ranges between 10 and 15 °C[16]. Layer 00 cooling is still under study, with the goal to keep silicon temperatures below approximately 5 °C in order to improve radiation resistance.

All components of the CDF II silicon system use port cards to receive data from and transfer control signals to the SVX3D readout chips. These port cards also regulate power to the hybrids and carry components that translate the SVX3D output

signals into optical format for transmission outside the tracking volume. They are mounted at the locations indicated in Figure 3. Since the port cards account for 35% of the total silicon system heat load of approximately 4 kW, they also receive active cooling.

## 6 DAQ

The data acquisition system for the CDF II silicon detectors is a fully pipelined DAQ+trigger architecture that can operate without downtime losses at machine bunch crossing intervals as low as 132 ns between cycles. A 42-cycle level-1 pipeline within each SVX3 chip permits storage of the analog signals for later digitization and transmission at rates up to 50 kHz. Almost all of the low-level data transmission between the port cards and the rest of the DAQ system occurs over optical fiber ribbons through a mixture of custom-manufactured and commercial boards and components.

An online trigger identifies displaced tracks at level 2, as described in reference [8]. This trigger will operate with  $\sim 20 \mu\text{s}$  latency at rates up to 300 Hz. It is followed in the data stream by a third level of software-based trigger processing that implements a portion of the offline analysis and reduces the final rate of logged events to less than 50 Hz. Further detail on the components and logic of the silicon DAQ system is contained in references [9], [10] and [17].

## 7 Assembly Plans and Expected Performance

Final assembly is in progress at the time of this writing for most of the silicon system components described above. Delivery of the silicon sensors should be complete by early to mid 2000, and assembly and testing of hybrids, ladders, and the DAQ system is currently in progress. Delivery of adequate quantities of the rad-hard SVX3D chip, however, has so far been somewhat constrained by problems in processing. Present plans call for a partially configured “fourth” barrel of the SVX II to be installed as early as possible to provide a test of hardware performance and to exercise the DAQ and trigger systems. This test barrel will be replaced by the full silicon system after applying any lessons learned from this early installation.

The expected impact parameter resolution of the full Run II CDF tracking system for minimum-ionizing particles is shown in Figure 10 versus transverse momentum of the normally-incident track. The grey shaded region shows the range of estimated resolution without the innermost layer, depending on whether or not the track passes through the region of the SVX II that contains its hybrid readout electronics. The line shows the improved resolution provided by the innermost layer. Without misalignments, the estimated intrinsic impact parameter resolution should improve from an average of  $\sigma_{IP} = (9 \oplus 50/p_T) \mu\text{m}$  for tracks at normal incidence without Layer 00 to an average of  $\sigma_{IP} = (6 \oplus 25/p_T) \mu\text{m}$

with the addition of this layer[9], for  $p_T$  in GeV/c. The values shown in Figure 10 include  $10 \mu\text{m}$  in quadrature as the estimated contribution of mechanical misalignments to the expected final resolution.

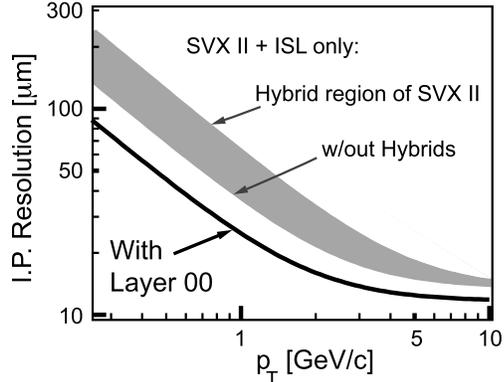


Fig. 10. Calculated impact parameter resolution at the location of the beam line for the CDF II silicon system.

Physics simulations of the full system show that the number of tracks and the signal-to-noise in displaced-vertex tags are also improved. The resulting efficiency for finding displaced vertices in  $b$  jets in top events is estimated to be 49% for single tags and 25% for double tags[9]. These numbers, which include geometric acceptances and are averaged over all top events, compare very favorably to the corresponding values of 25% and 8.0% for single and double tags with the SVX' vertex detector in Tevatron Run I, respectively.

## 8 Conclusions

The CDF Run II silicon vertex detector is a comprehensive upgrade that will provide substantially improved

performance in a large number of parameters over previous versions. The radiation hardness, geometric acceptance, pattern recognition capability and vertex finding efficiency, trigger compatibility, and readout speed are all either newly added or substantially improved. Upon completion, the resulting components should provide a tracking system of impressive capabilities that will add noticeably to the experiment's physics reach.

## References

- [1] F. Abe [CDF Collaboration], "The CDF detector: An overview," Nucl. Instrum. Meth. **A271**, 387 (1988), and references contained therein.
- [2] D. Amidei *et al.* [CDF Collaboration], "The silicon vertex detector of the Collider Detector at Fermilab," Nucl. Instrum. Meth. **A350**, 73 (1994); S. Cihangir *et al.*, "SVX-1: The new CDF silicon vertex detector," Nucl. Instrum. Meth. **A360**, 137 (1995).
- [3] F. Abe *et al.* [CDF Collaboration], "Measurement of the top quark mass and t anti-t production cross-section from dilepton events at the collider detector at Fermilab," Phys. Rev. Lett. **80**, 2779 (1998) hep-ex/9802017; F. Abe *et al.* [CDF Collaboration], "Observation of top quark production in anti-p p collisions," Phys. Rev. Lett. **74**, 2626 (1995) hep-ex/9503002.
- [4] F. Abe *et al.* [CDF Collaboration], "A Measurement of the lepton charge asymmetry in W boson decays produced in p anti-p collisions," Phys. Rev. Lett. **81**, 5754 (1998) hep-ex/9809001.
- [5] CDF II Collaboration, "The CDF II detector technical design report," Fermilab-Pub-96/390-E (1996).
- [6] D. Amidei *et al.*, "Electrical performance of the CDF silicon vertex detector," Nucl. Instrum. Meth. **A342**, 251 (1994); S.M. Tkaczyk, "Operational experience with CDF silicon microvertex detectors," Nucl. Instrum. Meth. **A368**, 179 (1995).
- [7] N. Bacchetta, D. Bisello, G. Bolla, C. Canali, P.G. Fuochi and A. Paccagnella, "Radiation effects on CDF AC coupled microstrip silicon detectors," Nucl. Instrum. Meth. **A326**, 381 (1993); P. Azzi *et al.*, "Radiation damage experience at CDF with SVX'," Nucl. Instrum. Meth. **A383**, 155 (1996); see also P. Derwent, these proceedings.
- [8] See the talk by Xin Wu, these proceedings, and A. Bardi *et al.*, "SVT: An Online silicon vertex tracker for the CDF upgrade," Nucl. Instrum. Meth. **A409**, 658 (1998).
- [9] The CDF II Collaboration, "Proposal for enhancement of the CDF II detector: An inner silicon layer and a time of flight detector," Fermilab-Proposal-909 (1998).
- [10] J. Antos *et al.*, "The SVX II silicon vertex detector upgrade at CDF," Nucl. Instrum. Meth. **A383**, 13 (1996); J. Antos *et al.*, "The SVX-II silicon vertex detector upgrade at CDF," Nucl. Instrum. Meth. **A360**, 118 (1995).
- [11] P. Azzi-Bacchetta *et al.* [CDF Collaboration], "The CDF intermediate silicon layers detector," to

be published in proceedings of 6th International Conference on Advanced Technology and Particle Physics, Villa Olmo, Italy, Oct 5-9, 1998.

- [12] T. Zimmerman *et al.*, “SVX3: A deadtimeless readout chip for silicon strip detectors,” Nucl. Instrum. Meth. **A409**, 369 (1998); M. Garcia-Sciveres *et al.*, “The SVX3D integrated circuit for deadtimeless silicon strip readout,” Nucl. Instrum. Meth. **A435**, 58 (1999).
- [13] S. Worm [CDF Collaboration], “Radiation effects in double sided silicon sensors for CDF,” Nucl. Instrum. Meth. **A418**, 120 (1998); A. Brandl, S. Seidel and S. Worm [CDF Collaboration], “Measurement of proton induced radiation damage effects in double sided silicon microstrip detectors,” Nucl. Instrum. Meth. **A399**, 76 (1997).
- [14] D. Bortoletto [CDF collaboration], “The CDF SVX II upgrade for the Tevatron run II,” Nucl. Instrum. Meth. **A386**, 87 (1997).
- [15] G. Bolla *et al.*, “Silicon microstrip detectors on 6” technology,” Nucl. Instrum. Meth. **A435**, 51 (1999).
- [16] P. Ratzmann, “Thermal analysis of the CDF SVX-II silicon vertex detector,” Nucl. Instrum. Meth. **A382**, 447 (1996).
- [17] M.C. Kruse [CDF Collaboration], “The Silicon tracking upgrade at CDF,” Proc. 3rd International Hiroshima Symposium on the Development and Application of Semiconductor Tracking Detectors, Melbourne, Australia, 9-12 Dec 1997.