17th International Conference
on Computing in High Energy and Nuclear Physics
Prague, 21-27 March 2009

The GigaFitter: Performances at CDF and Perspectives for Future Applications

Silvia Amerio
University of Padova & INFN

OUTLINE

The GigaFitter is a next generation **track fitter processor**.

→ Designed as a possible upgrade for CDF trigger system

→ Useful for future experiments

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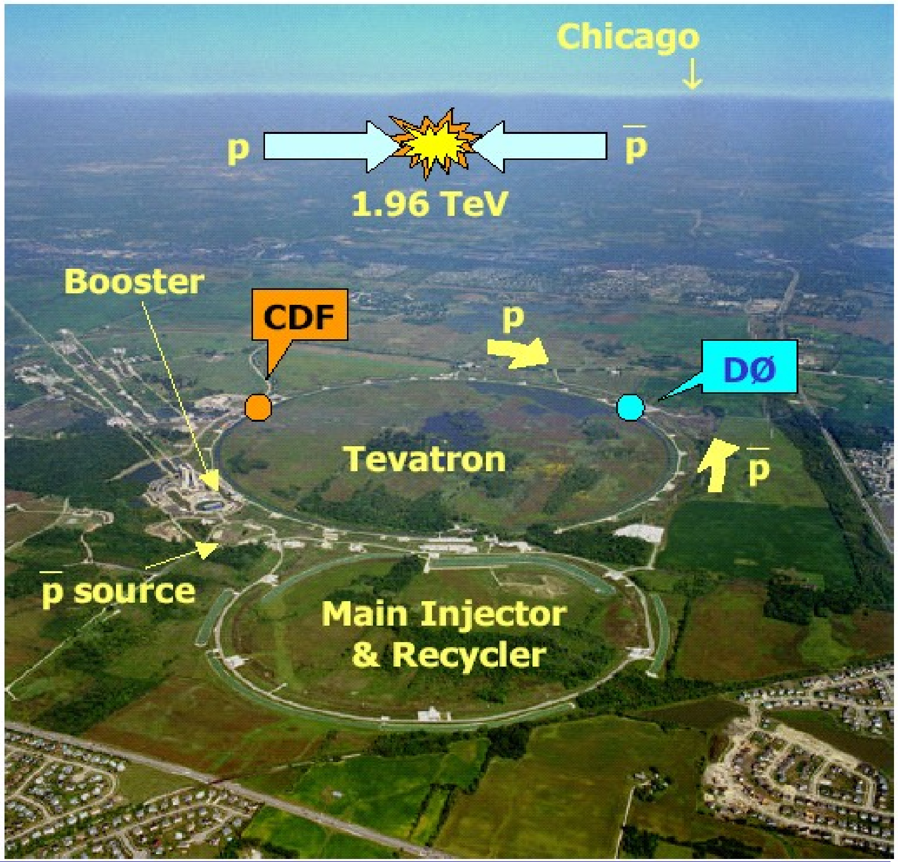
In this talk:

- CDF experiment and its trigger system
  - online track reconstruction (XFT and SVT)
- The Gigafitter:
  - implementation
  - advantages over current track fitter
  - current status
  - future applications

Tevatron accelerator
CDF experiment

Tevatron & CDF



CDF is a multipurpose detector

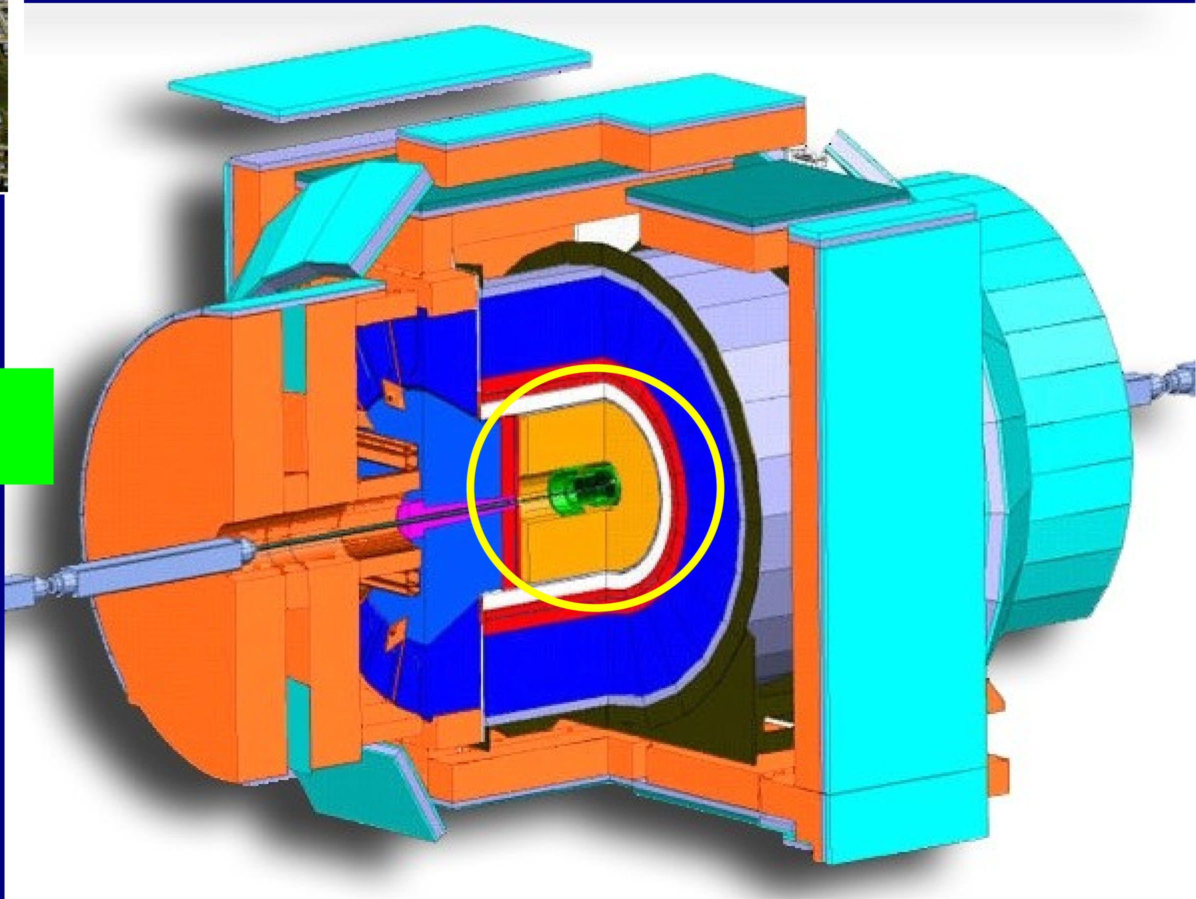
- charged particle tracking system
- calorimeters
- muon detectors

tracking system

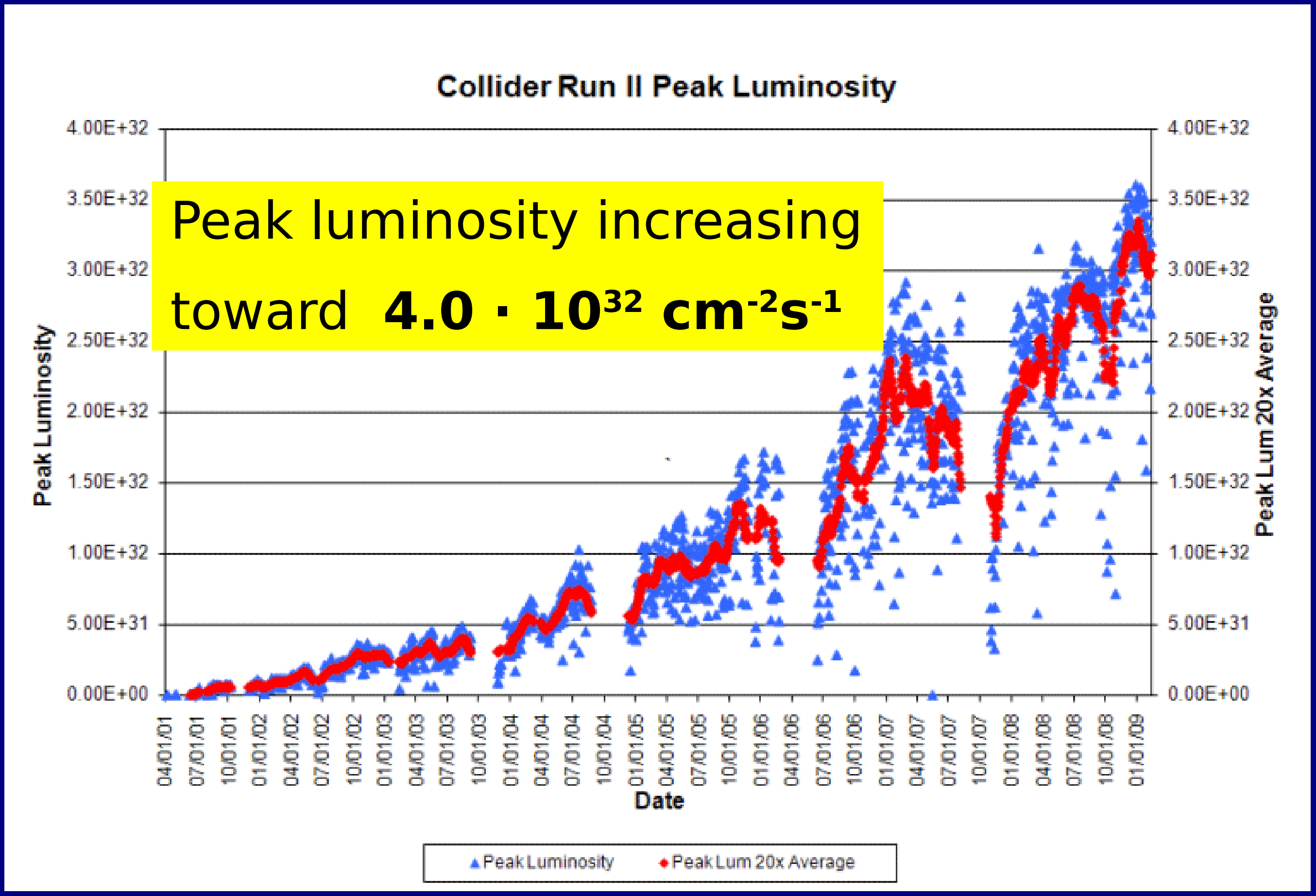
Silicon Vertex Tracker $(|\eta| < 2)$

- 5 layers of silicon microstrip detectors

Drift chamber $(|\eta| < 1)$



Tevatron performance



Drawback: more background and exponential increase in trigger rates

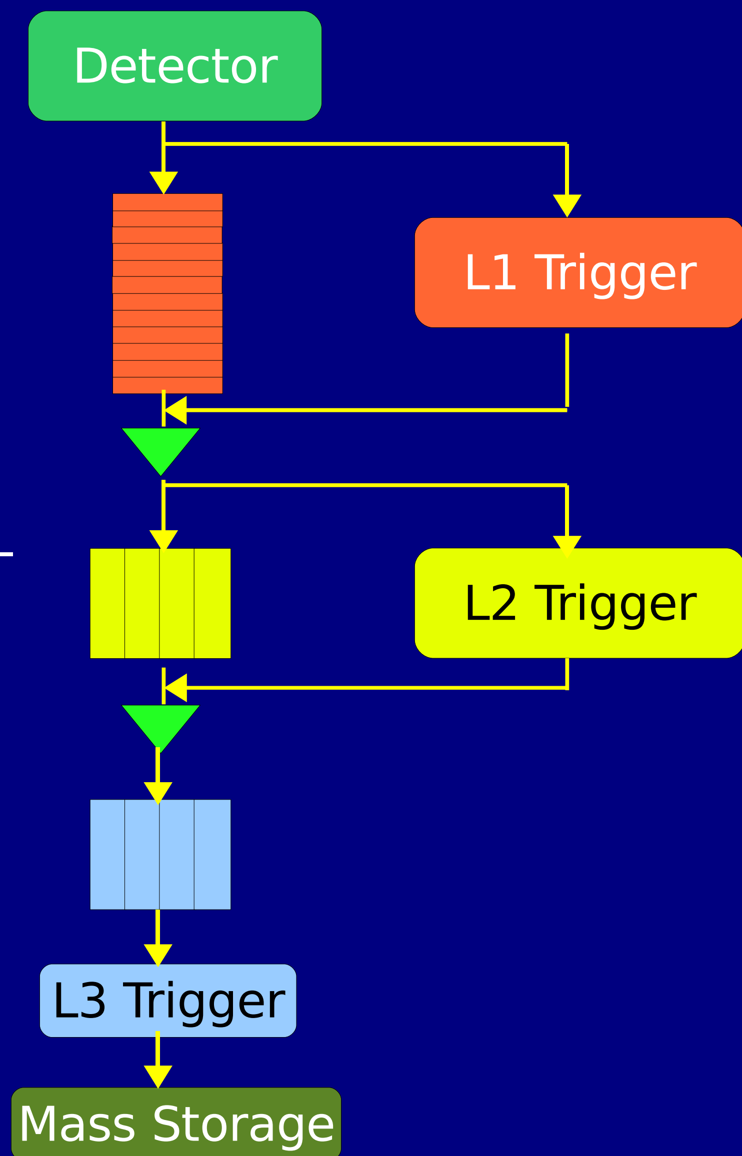
CDF trigger system flexible enough to be upgraded to cope with the increasing luminosity

Trigger system

2.53 MHz synchronous pipeline
Accept rate < 20 kHz

asynchronous 2-stages pipeline
Latency 20 μs
Accept rate < 1 kHz

PC farm
Accept rate < 100 Hz



At **each level** it can trigger on

- calorimetric objects
- muons
- **tracks**

reconstructed with increasing resolution

Online track reconstruction

- XFT
- SVT

XFT

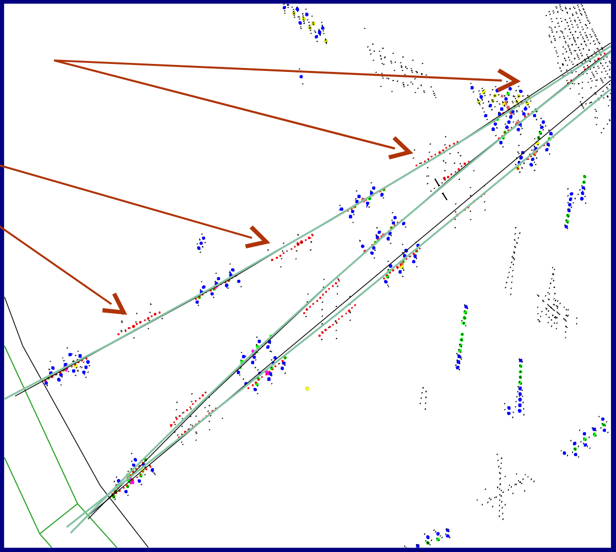
Level 1

Drift chamber hits → **EXtremely Fast Tracker (XFT) processor**

Finds tracks in the transverse plane of the drift chamber:

- 5.5 μs latency
- measures track p_T, ϕ, η and z

XFT segments

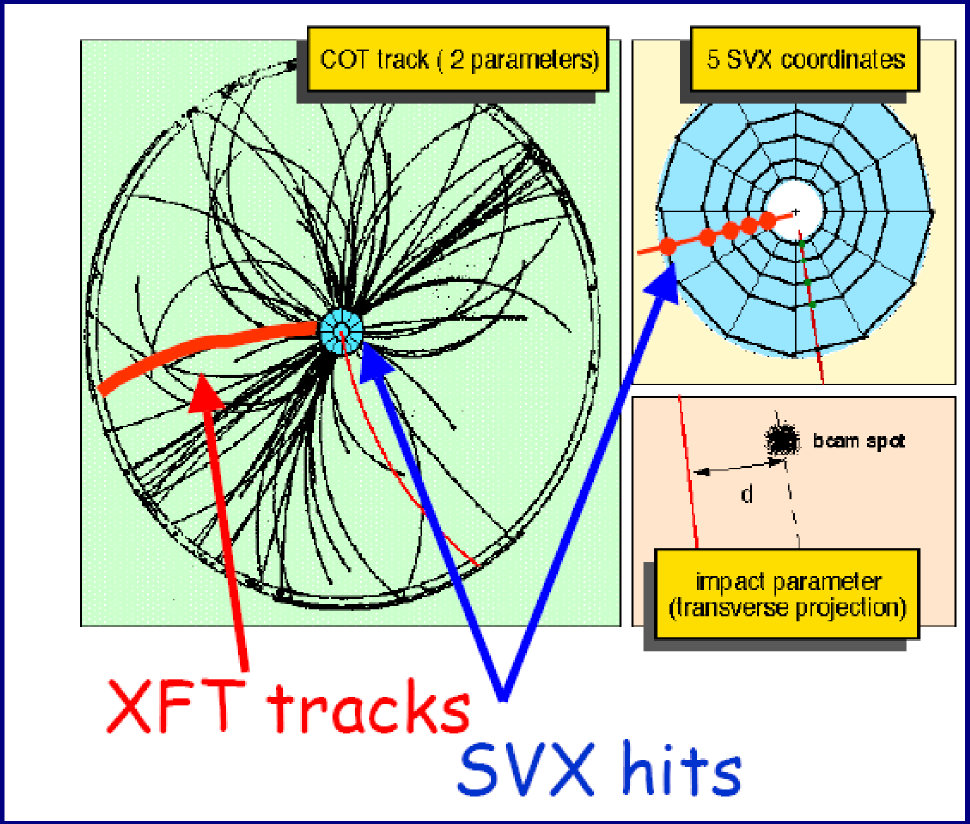


SVT

Level 2

XFT tracks
(p_T and ϕ) + **Silicon VerteX detector hits**

Silicon Vertex Trigger (SVT) processor



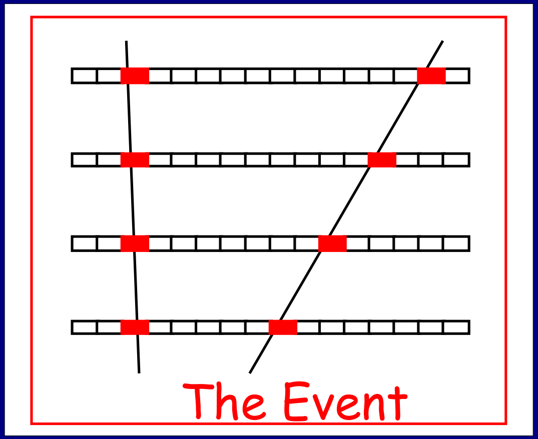
- output: **curv**, ϕ, $\mathbf{d_0}$, χ^2
- 20 μs latency
- offline-like resolution

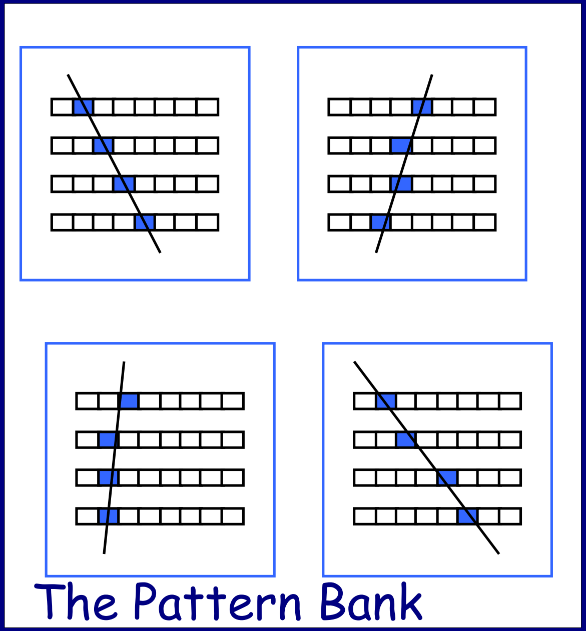
(35 μm on d_0)

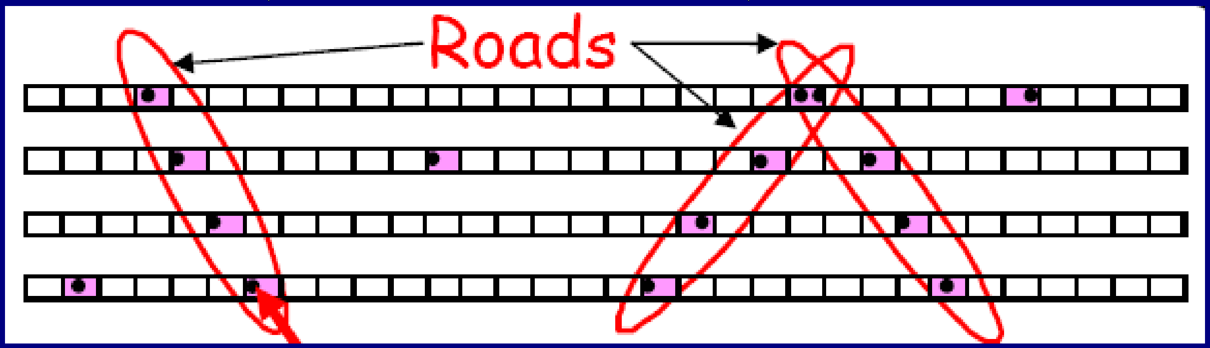
A two step algorithm

SVT - 1st Step: Pattern Recognition

PATTERN RECOGNITION
(by Associative Memory)







Finds **low resolution track candidates (roads)**

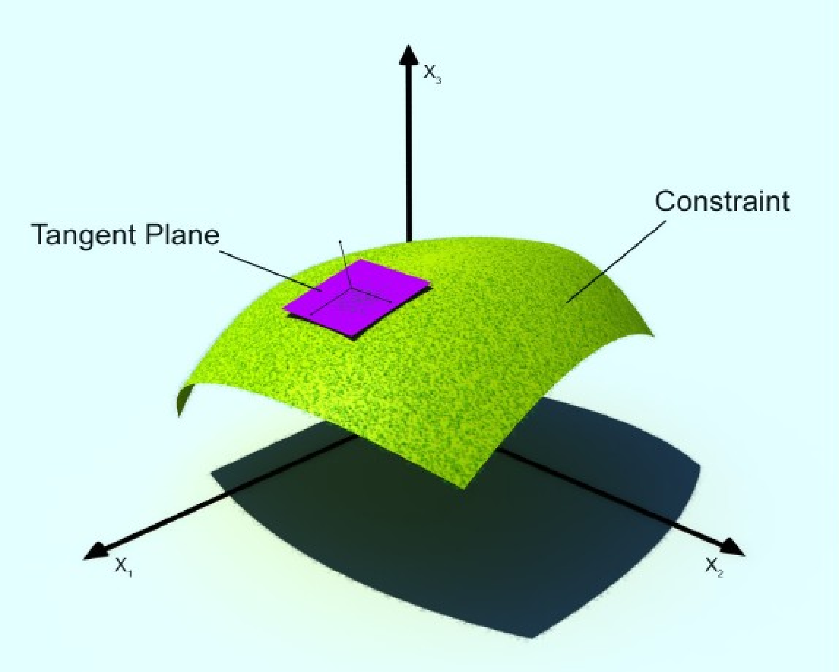
SVT - 2nd Step: Track Fitting

TRACK

defined by 6 coordinates x_i
(4 SVX hits + p_T and ϕ from XFT)

described by 3 parameters
(**curv, ϕ and d_0**)

3 constraint functions that can be locally (within a road) linearized



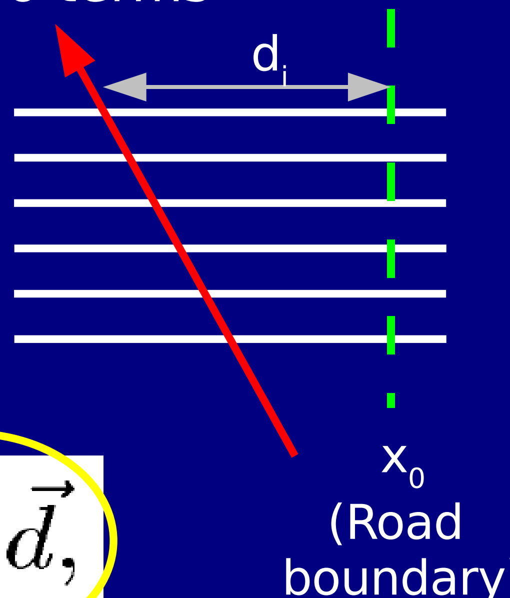
$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$

p_i = track parameters to be fitted
$\mathbf{x}_i$ = track coordinates
$\mathbf{f}_i$, q_i = known costants

SVT implementation and limits – I

Track coordinate = **18 bits**
TF multipliers = **8 x 8 bits**

→ scalar product has to be splitted in two terms



$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$

$$p0_i + \delta p_i = (\vec{f}_i \cdot \vec{x}_0 + q_i) + \vec{f}_i \cdot \vec{d},$$

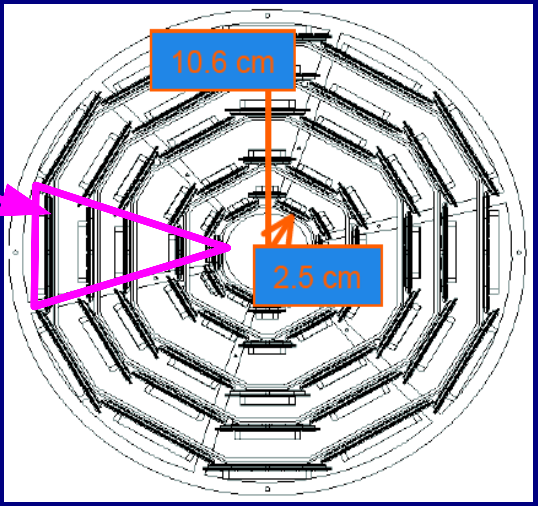
precalculated (one for each road), stored in **large memories**

online evaluated with 8x8 multipliers

SVT implementation and limits – II

SVX is organized in 12 ϕ sectors (wedges), 30° each

12 TF boards



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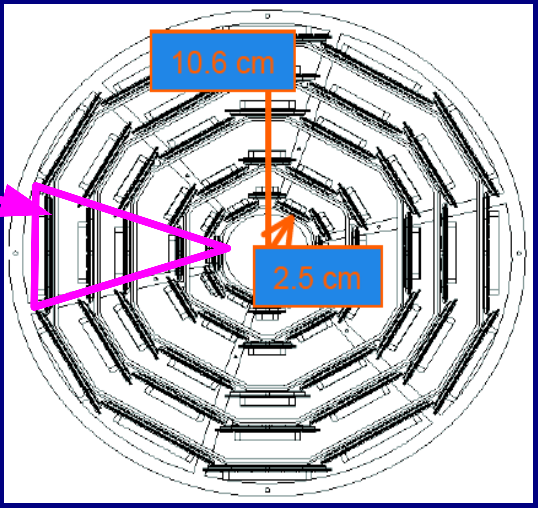

12 TF boards

Patterns are precomputed offline → **512 k roads / SVX sector**
The number of patterns is **limited**

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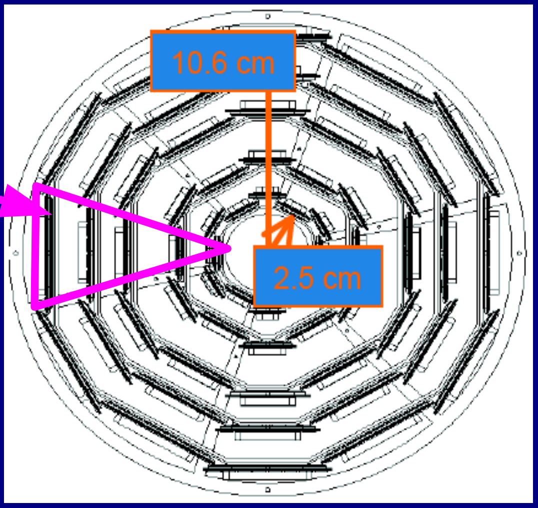
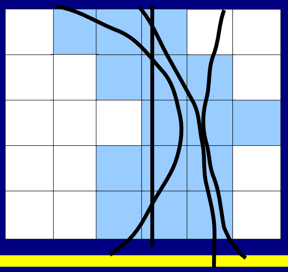


Patterns are precomputed offline → **512 k roads / SVX sector**
The number of patterns is **limited**

Road size is **200 µm**

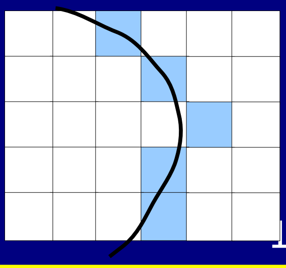
if larger →

- greater efficiency
- many tracks to fit
- high processing time



if smaller →

- small processing time
- efficiency limited by the max # of patterns



The Gigafitter

The GigaFitter

- Designed as a possible replacement of the current Track Fitter
- Can overcome the SVT limits and increase SVT performances at high luminosity

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Based on modern FPGA

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Provided with **640 DSP**

- 25 x 18 bit multipliers
- 48 bit adders

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Thanks to Xilinx for kind donation!

Based on modern FPGA

Xilinx VIRTEX 5 : 65 nm – 550 MHz device

Provided with **640 DSP**

- 25 x 18 bit multipliers
- 48 bit adders

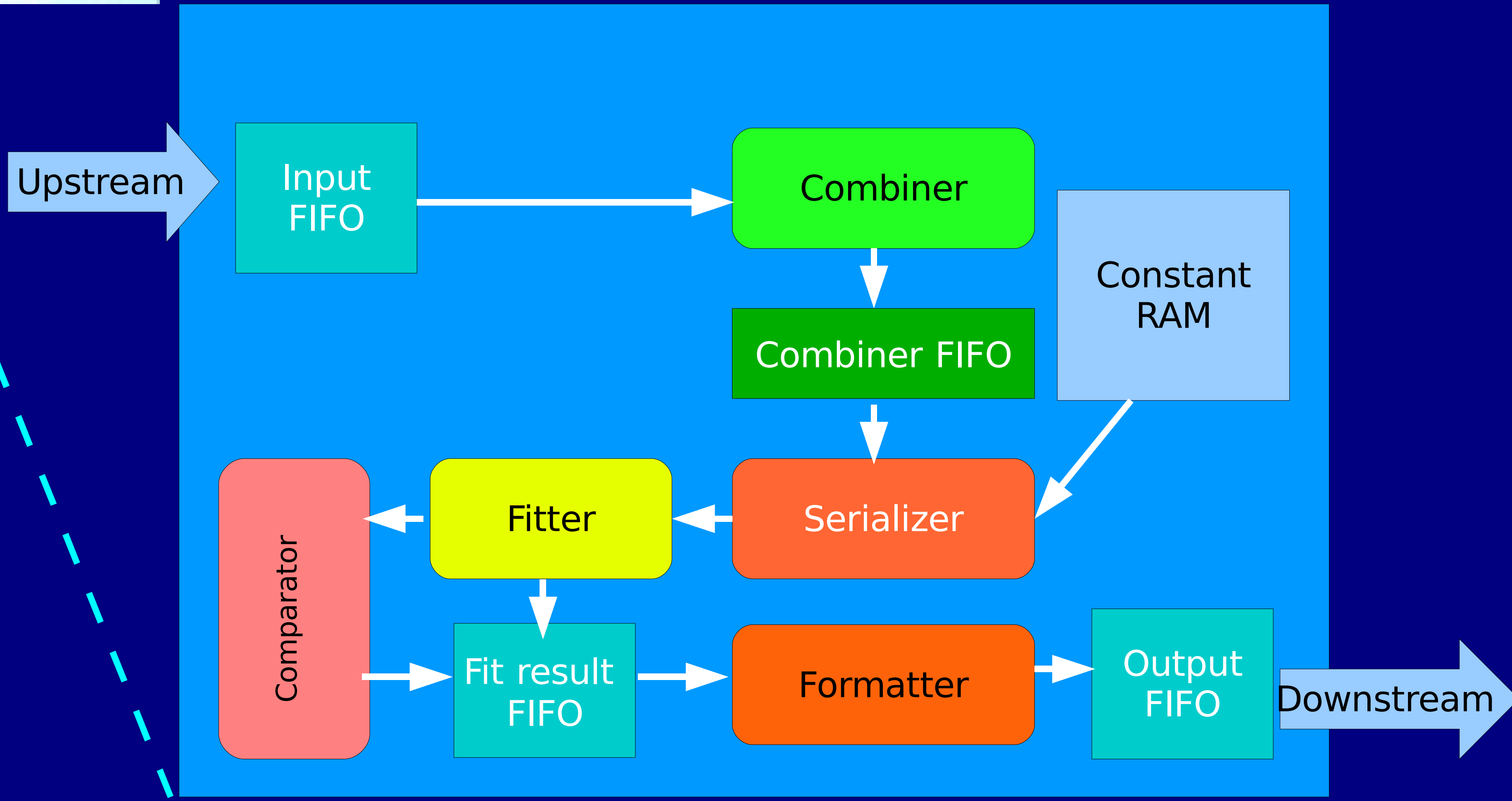
Can use full hit resolution → 18 x 18 multipliers, no need for precalculated terms stored in big memories

Memory available to store **more patterns and more constant sets!**

The Gigafitter

Implementation

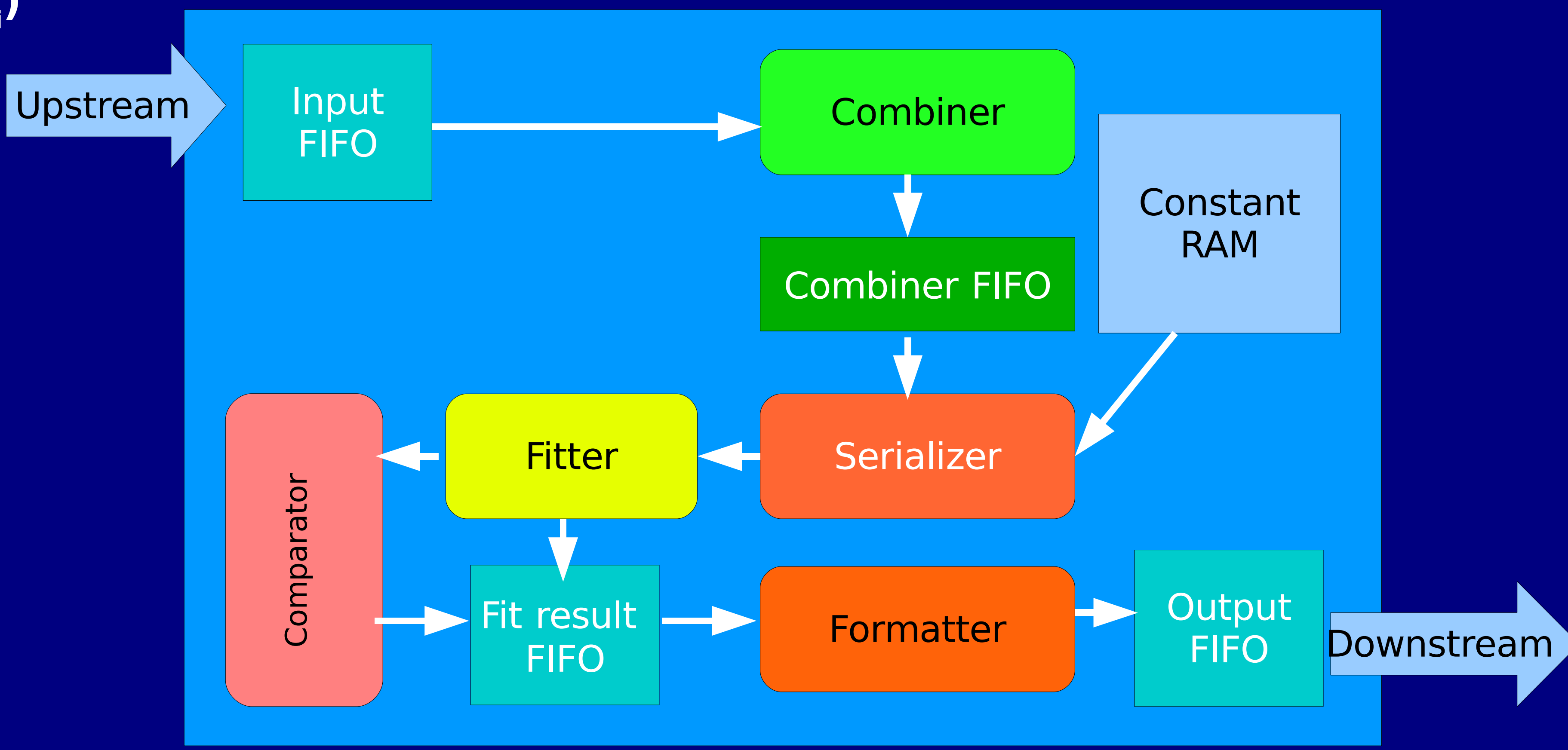
GF basic fit line



GF basic fit line

$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$

SVX hits
+
XFT p_T and ϕ
(x_i)



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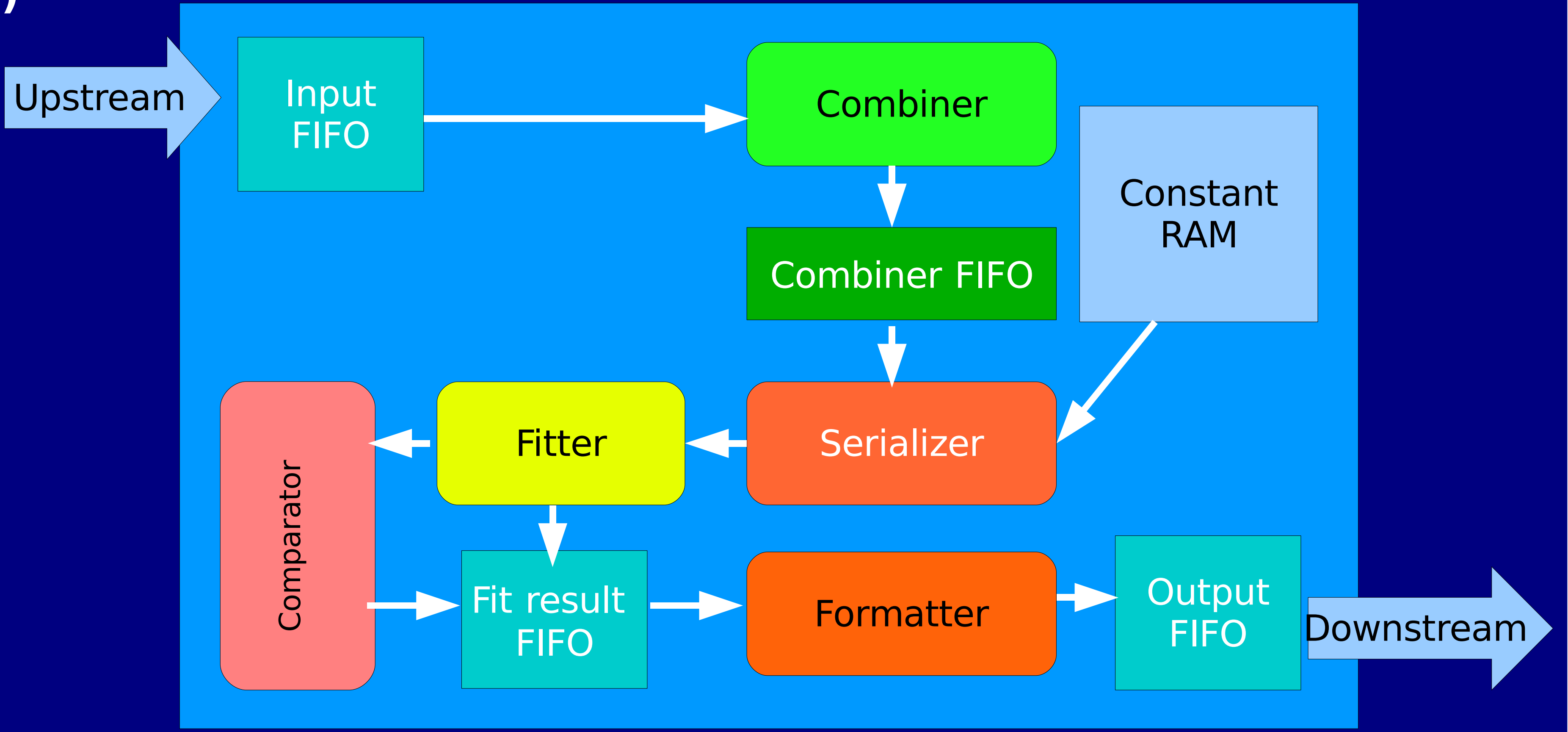
Multiple hits in the same SVX layer → do all the combinations



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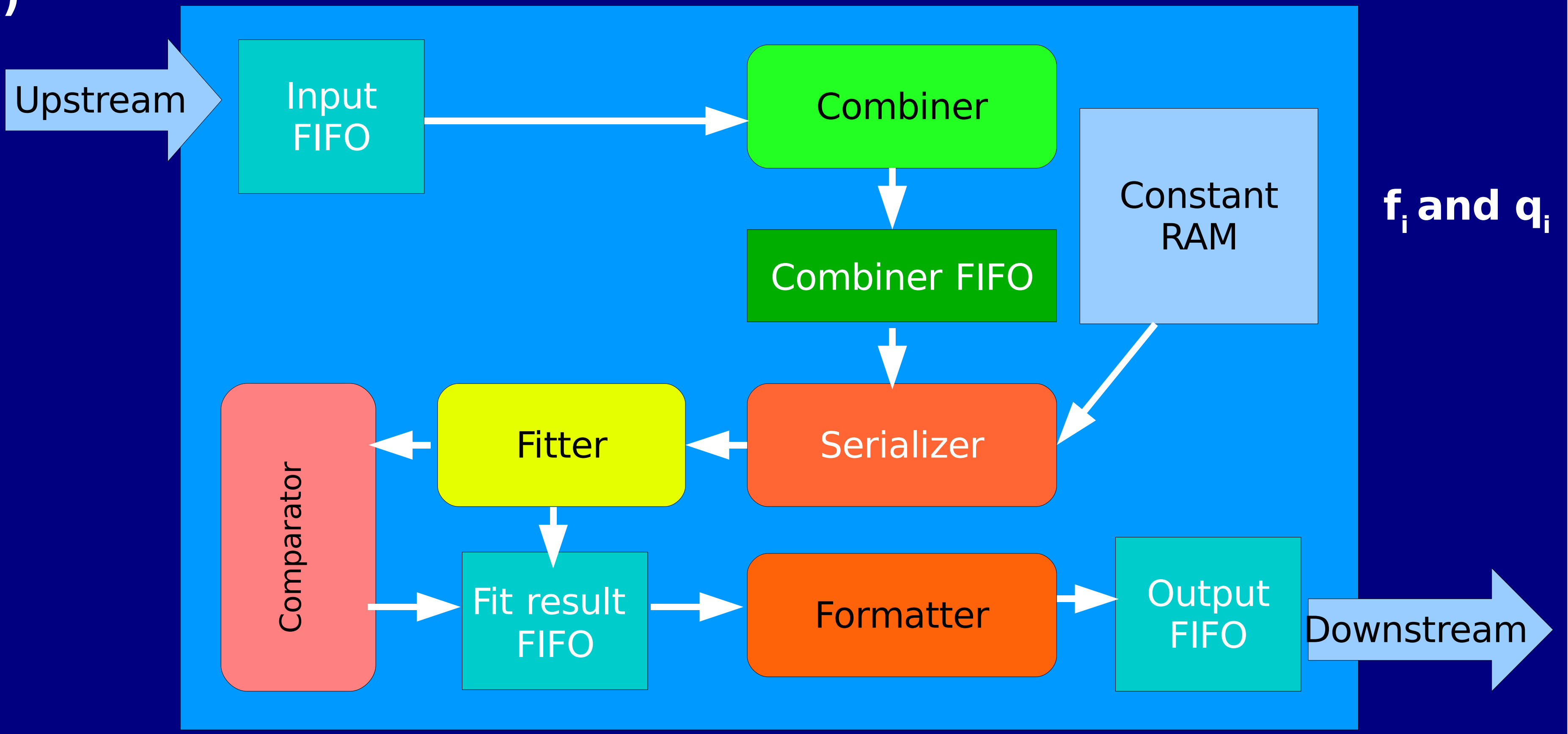
$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$

SVX hits + XFT p_T and ϕ (x_i)

Multiple hits in the same SVX layer → do all the combinations



f_i and q_i

GF basic fit line

$$p_i = \vec{f}_i \cdot \vec{x} + q_i$$

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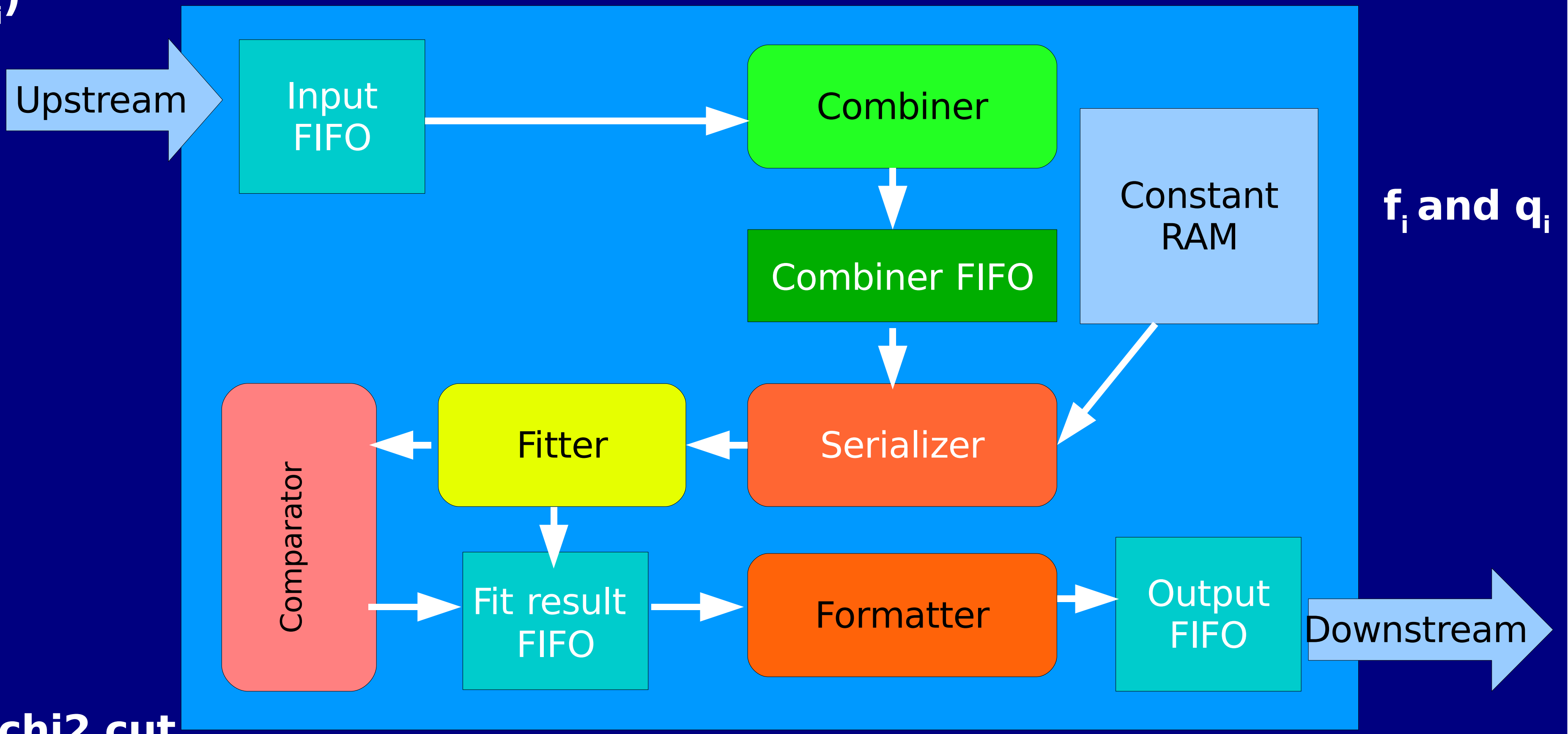


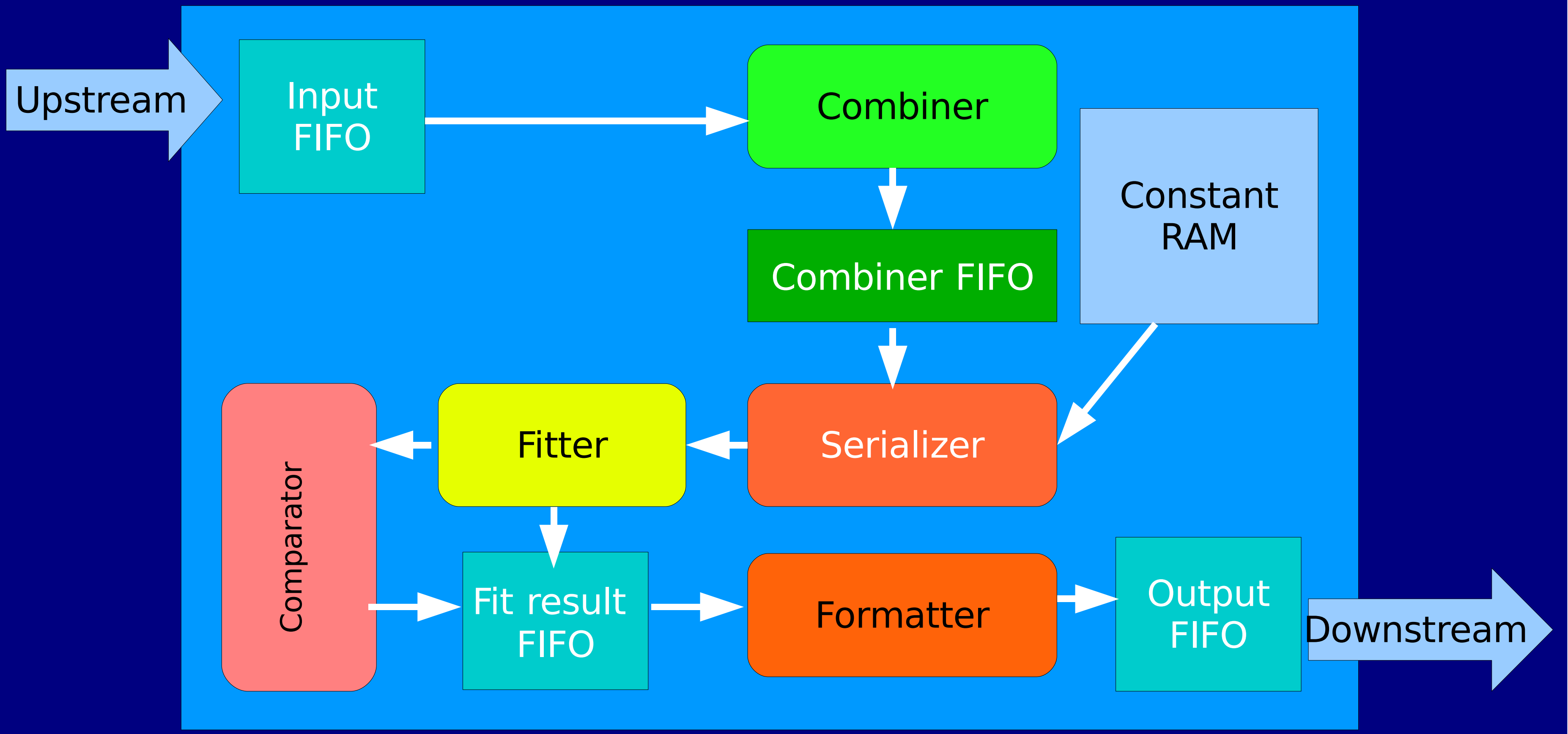
f_i and q_i

- **apply chi2 cut**
- **select the *best* track**

7 DSP used
1 fit every 6 clock cycles

GF optimization

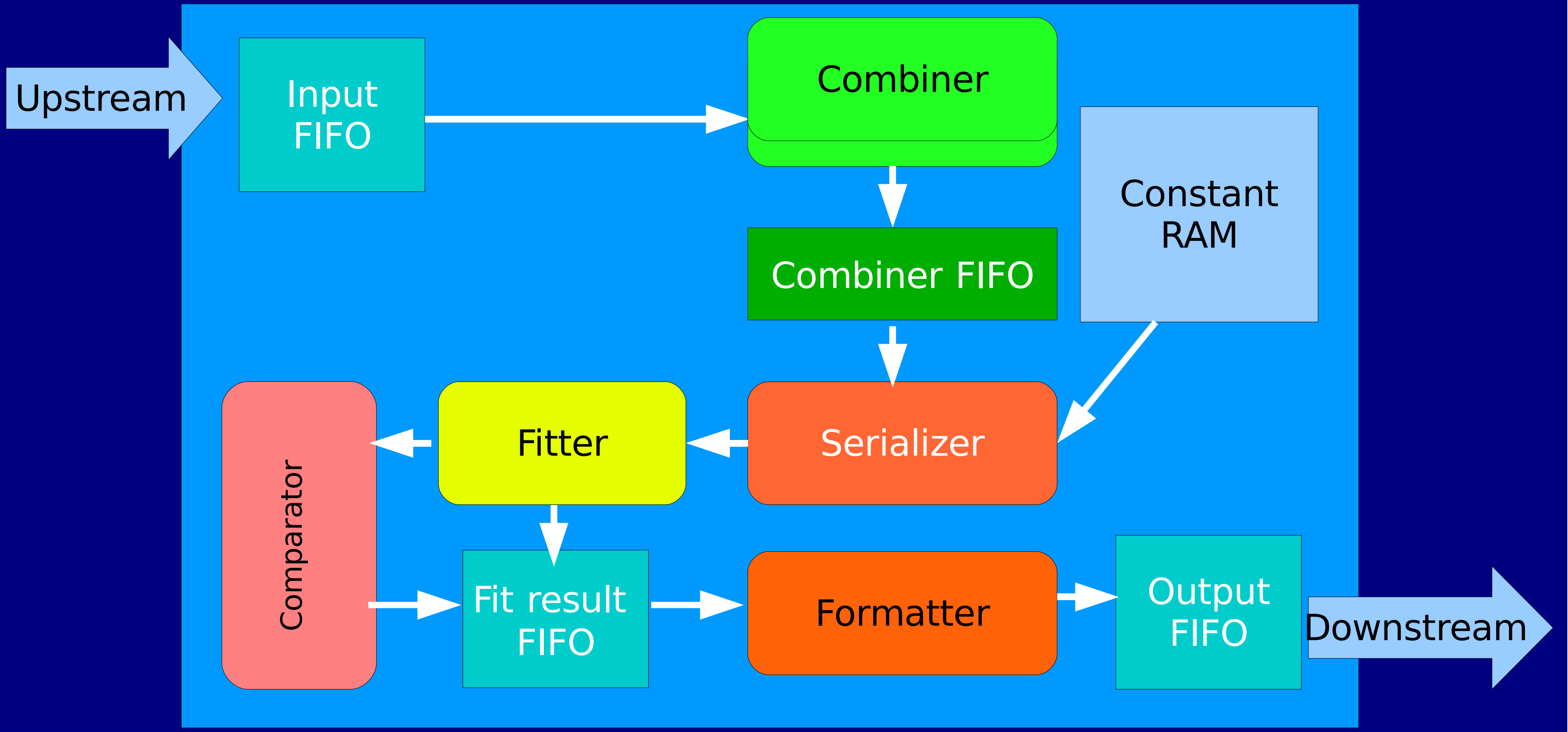
GF processing time can be reduced parallelizing the tasks



GF optimization

GF processing time can be reduced parallelizing the tasks

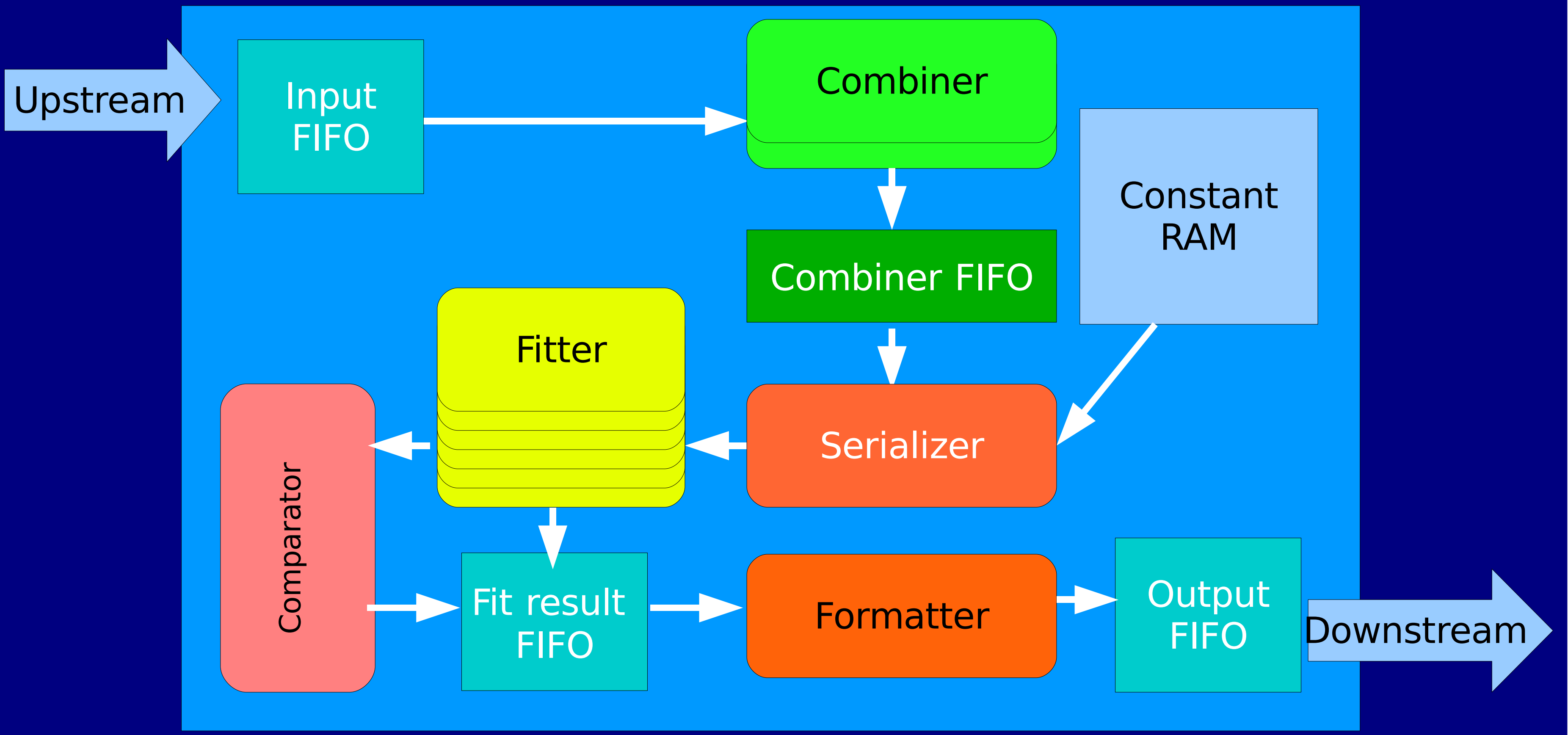
Combiner: ≥ 7 clock cycles to read, ≥ 3 to write
→ at least 2 parallel COMBINERS for continuous read/write



GF optimization

GF processing time can be reduced parallelizing the tasks

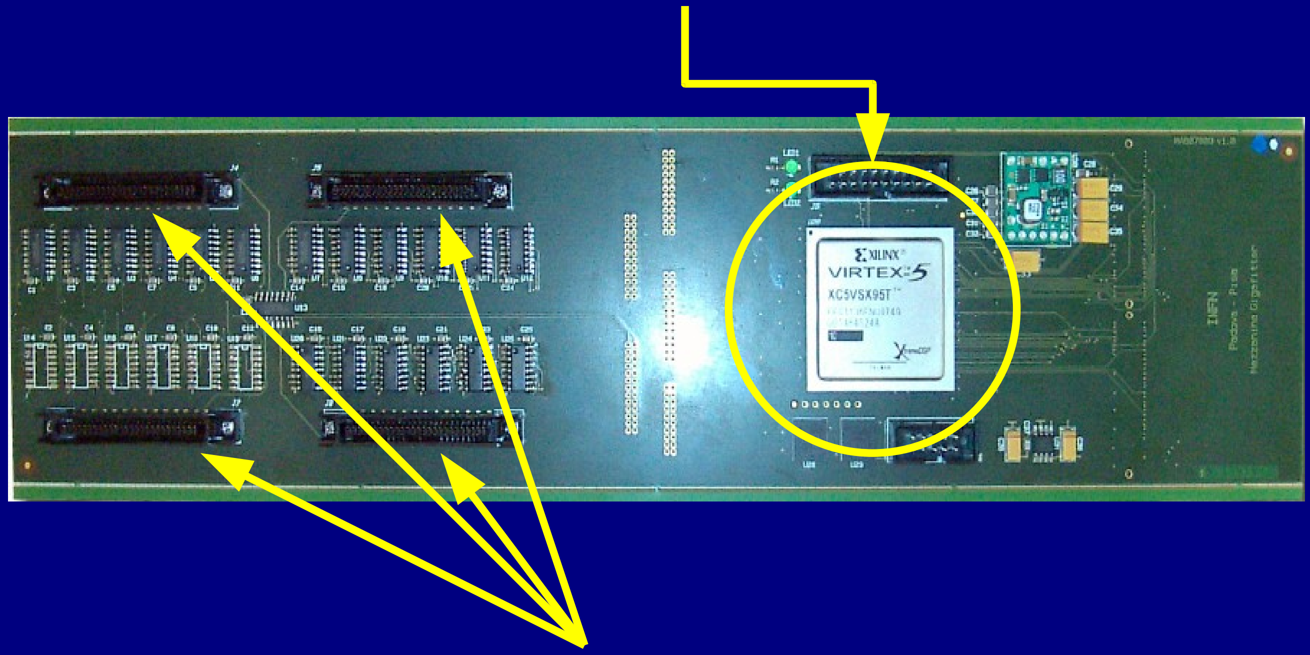
Fitter: 6 clock cycles to perform a scalar product
→ up to 6 parallel FITTERS to achieve 1 fit/clk



42 DSP used
1 fit every clock cycle

Mezzanine card

Xilinx VIRTEX 5 is mounted on a mezzanine card



Each mezzanine receives the inputs from 4 out of 12 SVX wedges

Virtex 5:
640 DSP → 160 DSP per SVX wedge → up to 3 fit lines per wedge
(1 fit line = 6*7 = 42 DSP)

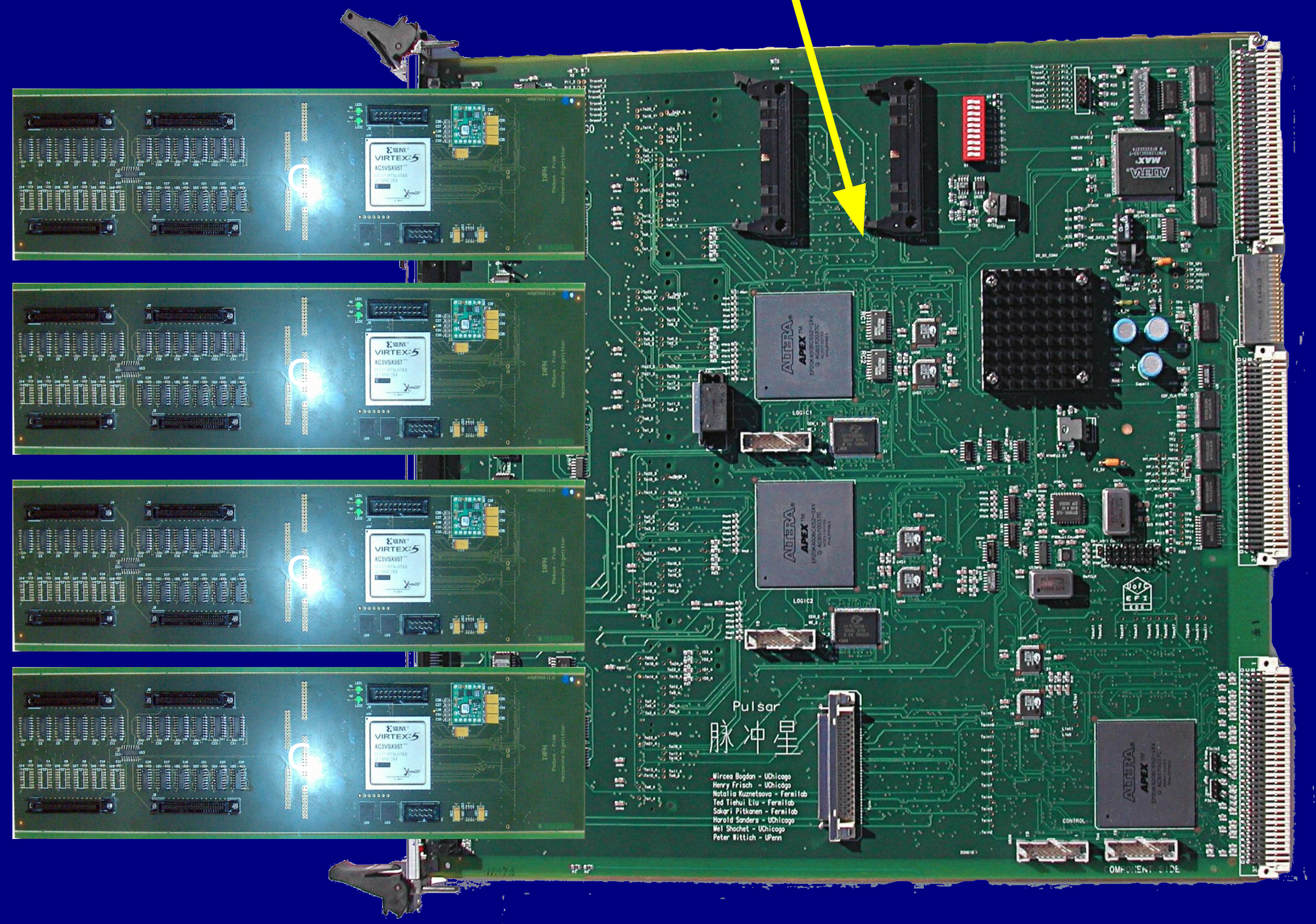
High level of parallelization, high speed

Final system

PULSAR board
general purpose 9U VME interface board

12 SVX wedges

RAM



GF = 1 board ⟷ **Current system = 16 boards (12 TF + 4 merger boards)**

The Gigafitter

Advantages over current track fitter

Where do we gain? - I

SPEED Necessary in a very high luminosity scenario

3 mezzanines,
4 wedges each,
3 fit lines per wedge

up to **36 fits / clock cycle**
(**3 fits/ns** at 100 MHz internal clock)

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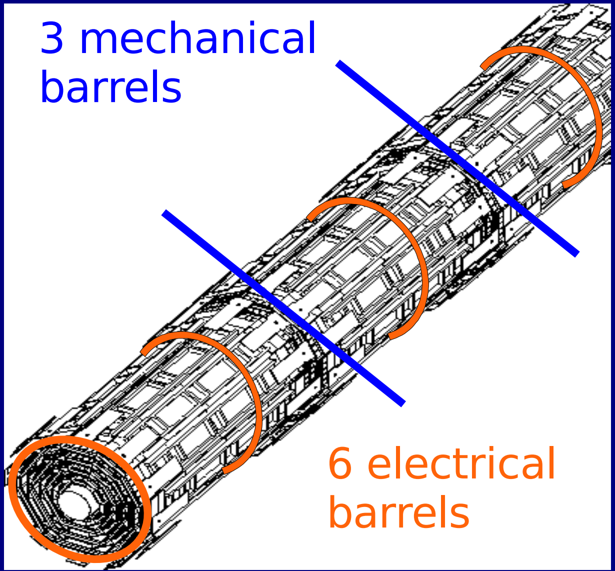
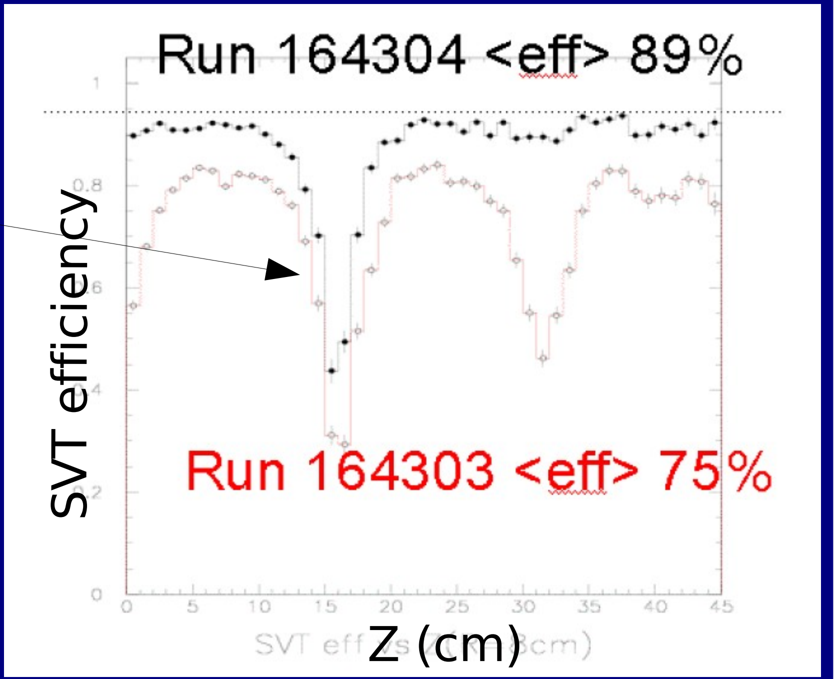
SVT Acceptance

Greater available memory → more patterns!

Eg.: can include patterns for tracks crossing the mechanical barrels of SVX



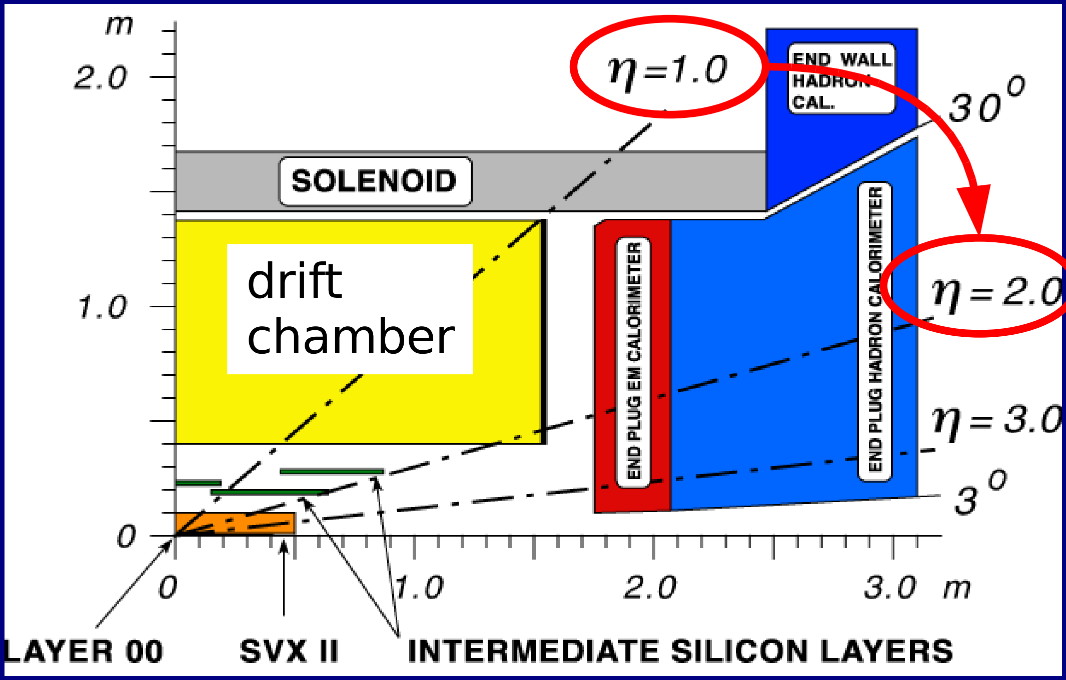


Where do we gain? - II

SVT Acceptance

Greater available memory
→ include patterns for

- silicon only tracks for a larger eta coverage

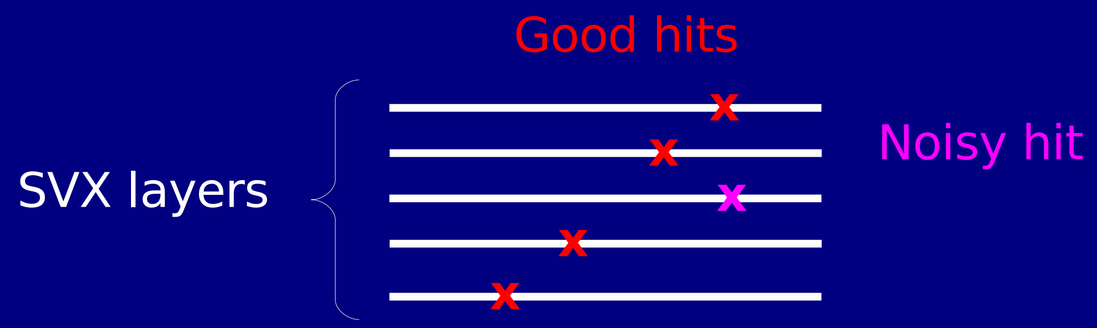


Useful to trigger on forward electrons, muons and taus.

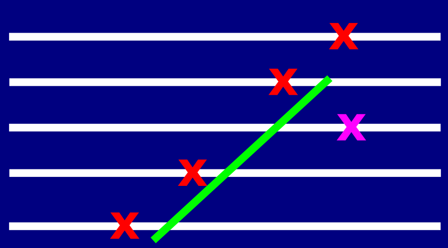
Important to increase Higgs acceptance.

Where do we gain? - III

SVT Efficiency



Track Fitter



Bad χ^2

Track rejected

GigaFitter

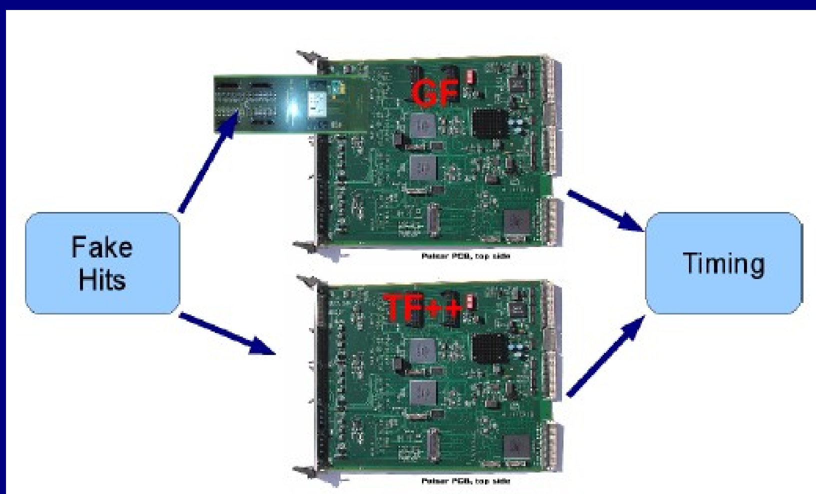
Fit all possible combinations of 4 hits and select the best

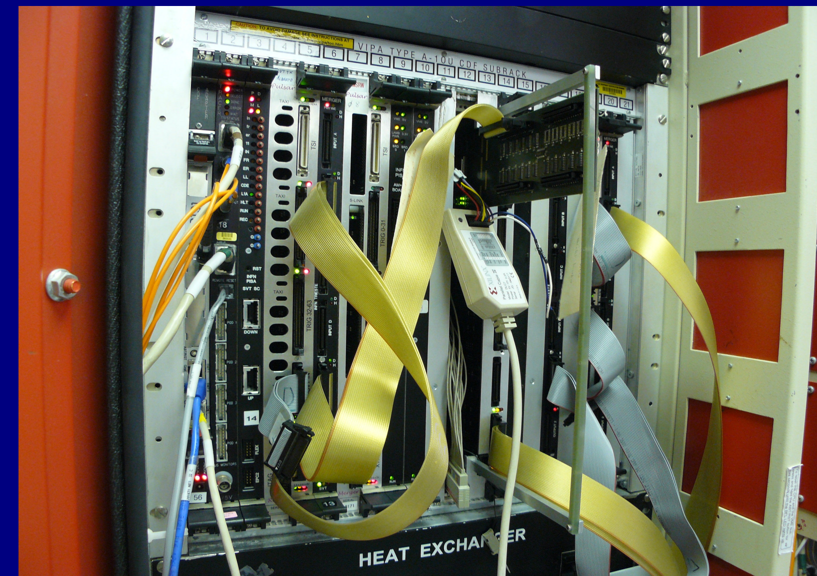
The Gigafitter

Current status

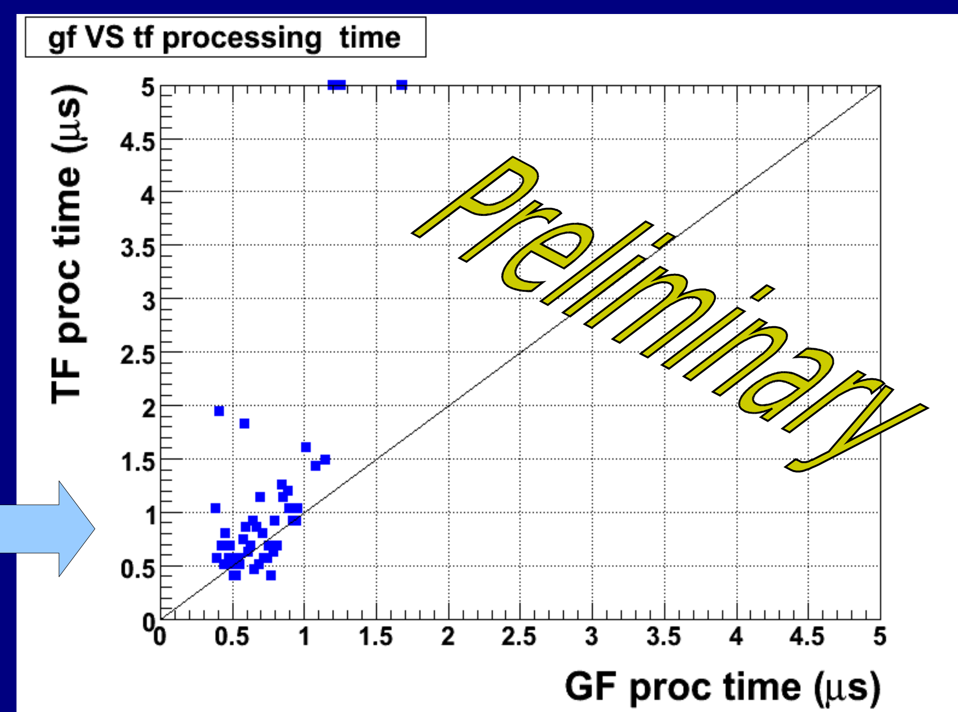
GF current status

1 mezzanine on a pulsar board installed and tested in parasitic mode for preliminary timing measurements





GF with 1 fit line w/o parallelism
1 fit every 6 clock cycles at 120 MHz



The Gigafitter

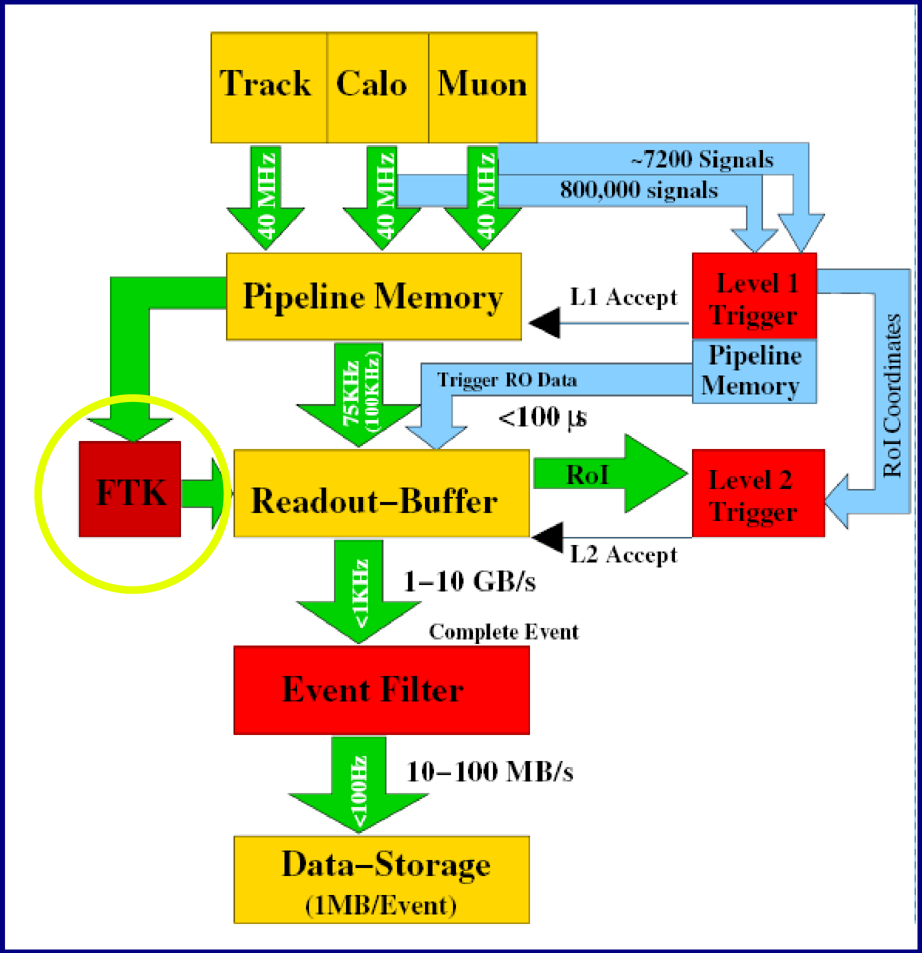
Future applications

Future applications

Gigafitter type tracking processor can be used in future online tracking processors for high-quality track finding at very high rates.

FTK (Fast Track) is a proposal for a SVT-like tracking processor at ATLAS Level 2 trigger

It is intended to provide offline quality tracks for all particles w/ $p_T > 1$ GeV, up to 50 - 100 kHz of L1 rate



IEEE Trans. Nucl. Sci. 51, 391 (2004)
IEEE Trans. Nucl. Sci. 55, 145 (2008)

Summary

The **GigaFitter** is an online tracking processor developed as a *possible upgrade of CDF trigger system*, following the successful strategy implemented by the **SVT processor**.

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Based on a modern FPGA provided of *many DSP arrays*, it features

- **high computation power**
- **high flexibility and modularity**

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The **GigaFitter** is an online tracking processor developed as a *possible upgrade of CDF trigger system*, following the successful strategy implemented by the **SVT processor**.

Based on a modern FPGA provided of *many DSP arrays*, it features

- **high computation power**
- **high flexibility and modularity**

At CDF it will allow to

- *reduce trigger dead time and rate* at high instantaneous luminosity
- improve the physic reach (*increased track reconstruction efficiency*)

Summary

The **GigaFitter** is an online tracking processor developed as a *possible upgrade of CDF trigger system*, following the successful strategy implemented by the **SVT processor**.

Based on a modern FPGA provided of *many DSP arrays*, it features

- **high computation power**
- **high flexibility and modularity**

At CDF it will allow to

- *reduce trigger dead time and rate* at high instantaneous luminosity
- improve the physic reach (*increased track reconstruction efficiency*)

But it can also be **adapted to future experiments** inside (i.e.LHC) and outside HEP

BACKUP

CDF Detector

tracking system immersed in a

solenoid coil

Silicon Vertex Tracker ($|\eta| < 2$)

Drift chamber ($|\eta| < 1$)

calorimeters ($|\eta| < 3.6$)

electromagnetic

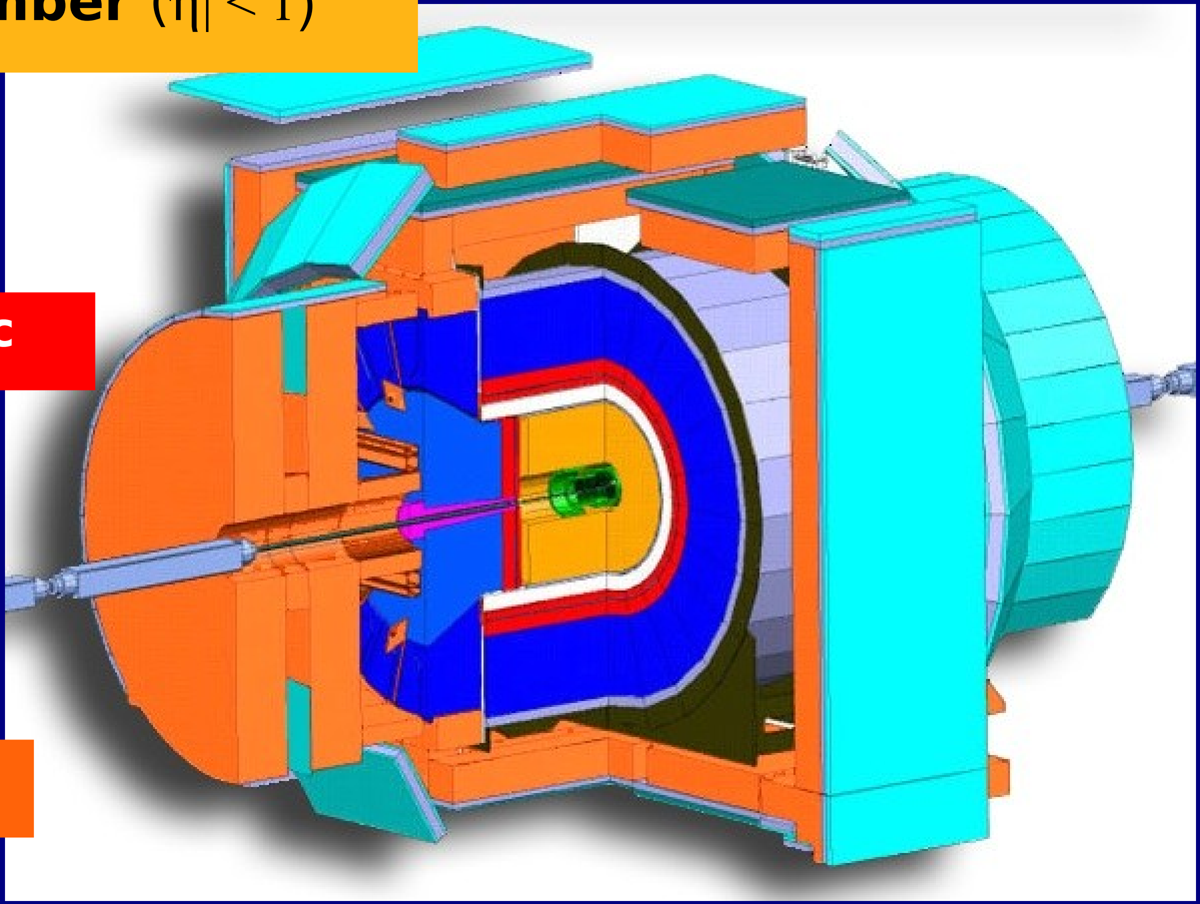
hadronic

muon detectors ($|\eta| < 1.1$)

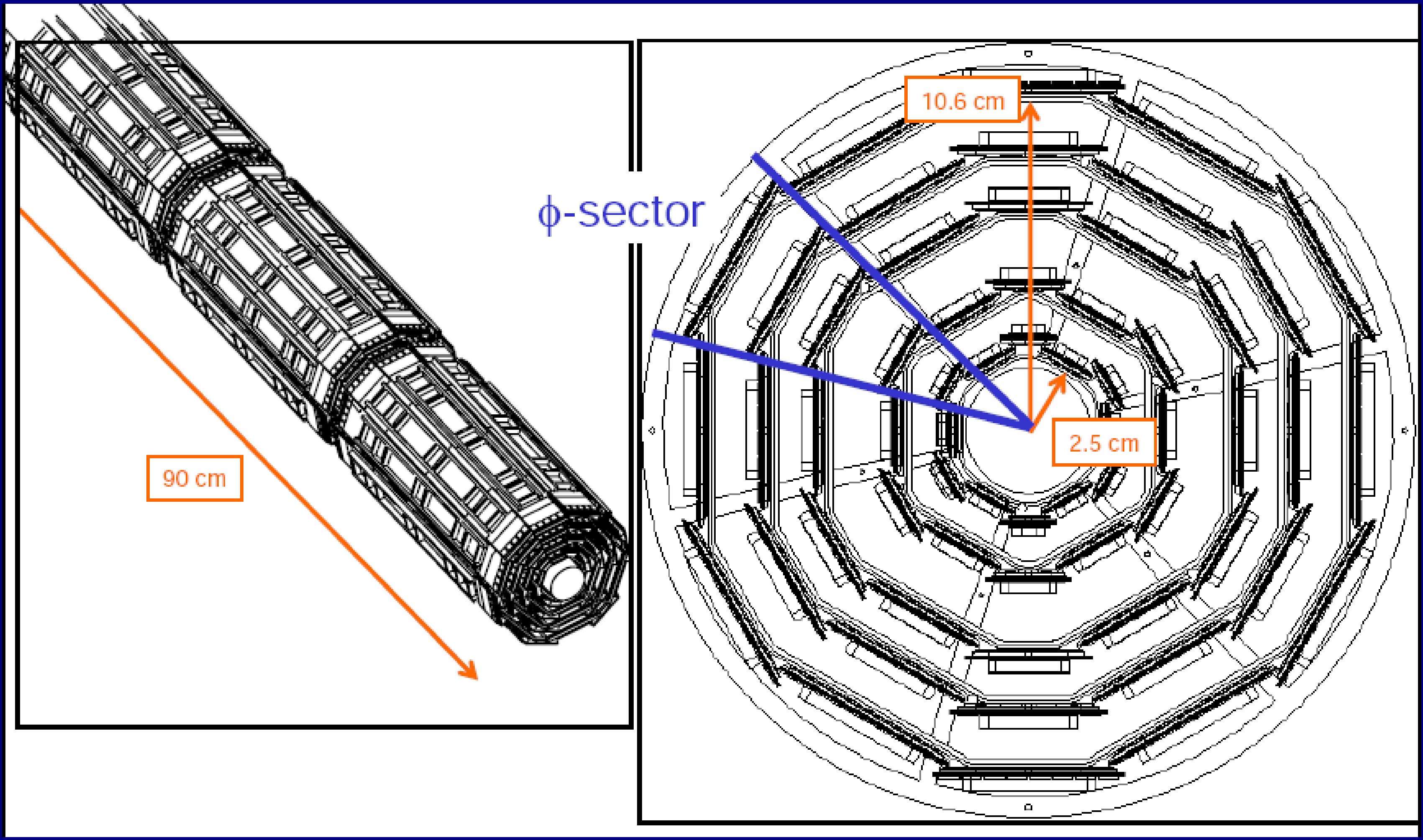
drift chambers

scintillators

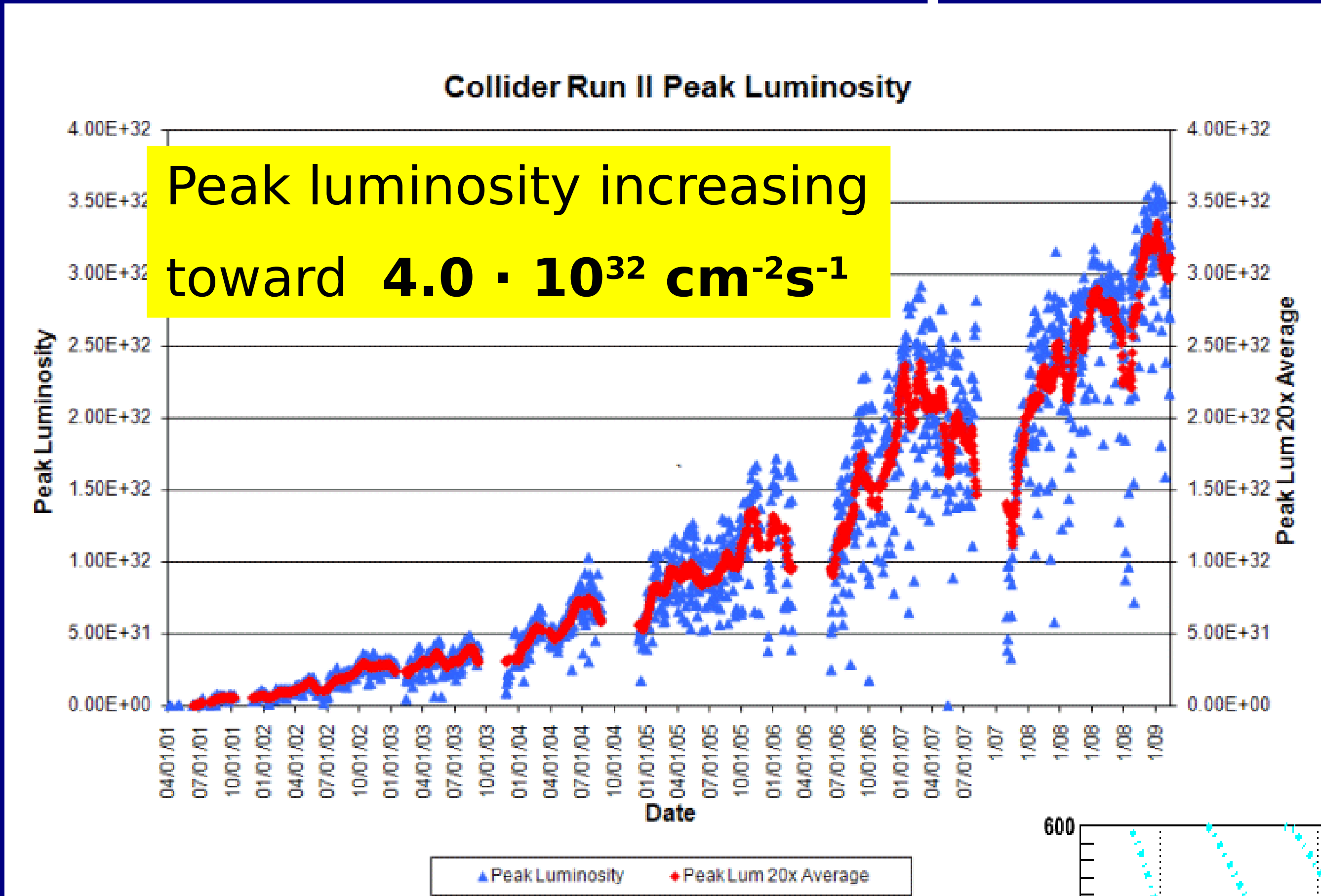
steel shielding



SVX



Tevatron performance



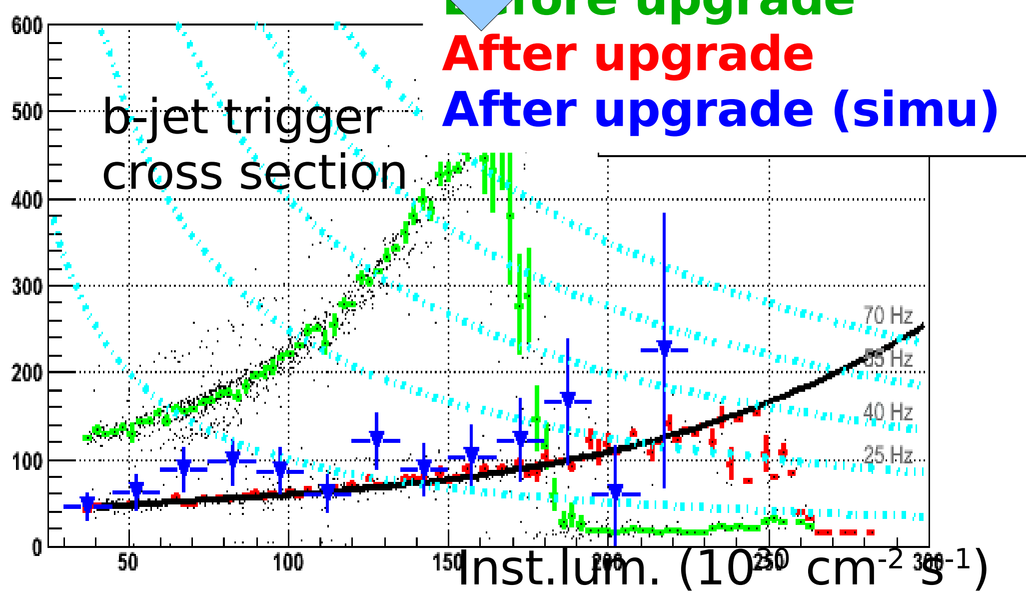
Peak luminosity increasing toward **$4.0 \cdot 10^{32}$ cm^{-2}s^{-1}**

Drawback: more background and exponential increase in trigger rates

Before upgrade

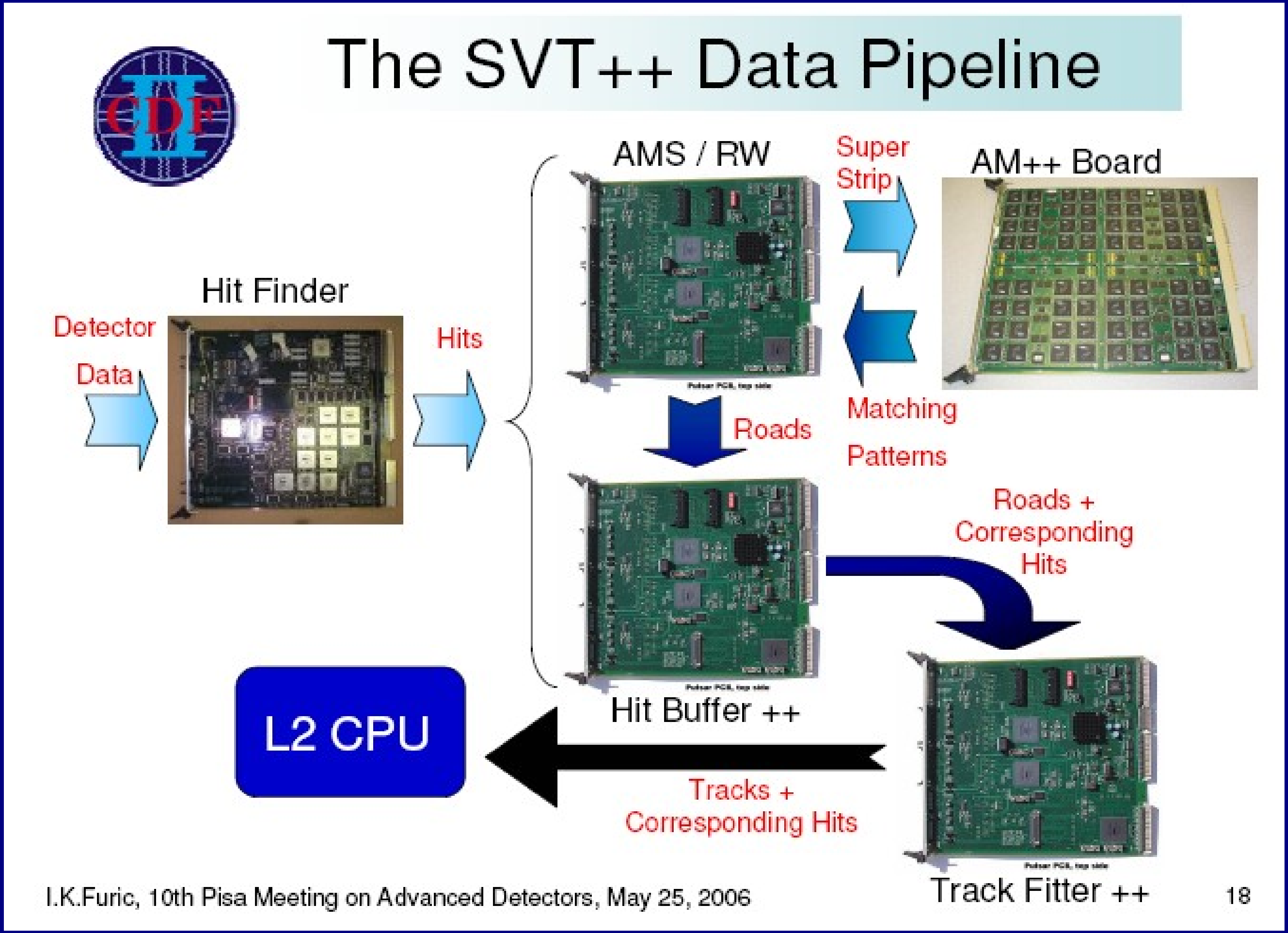
After upgrade

After upgrade (simu)



CDF trigger system flexible enough to be upgraded to cope with the increasing luminosity

SVT


The SVT++ Data Pipeline
AMS / RW
Super Strip
AM++ Board
Hit Finder
Detector Data
Hits
Roads
Matching Patterns
Roads + Corresponding Hits
Hit Buffer ++
L2 CPU
Tracks + Corresponding Hits
Track Fitter ++
I.K.Furic, 10th Pisa Meeting on Advanced Detectors, May 25, 2006
18

XFT and SVT resolutions

XFT

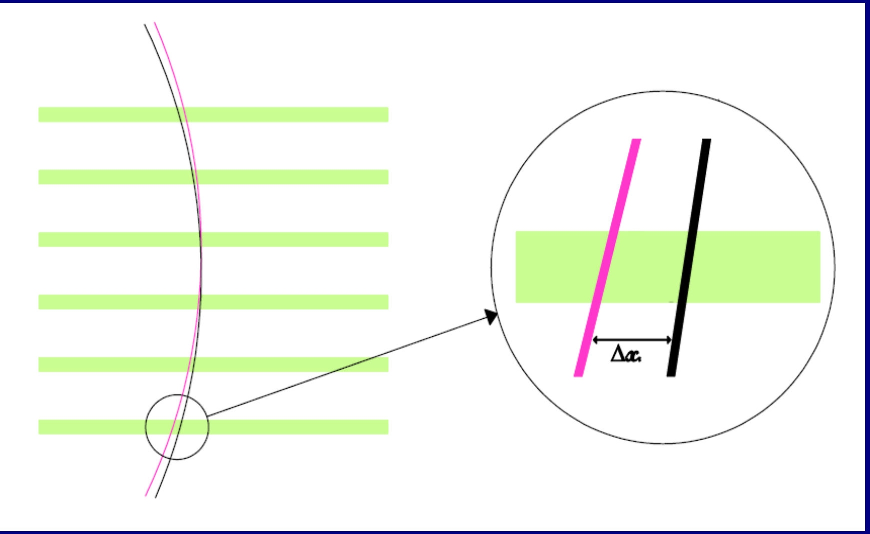
- eff > 96% (p_T > 1.5 GeV)
- $\sigma_{pT}/p_T^2 \sim 2\%$
- $\sigma_\phi \sim$ 2 mrad
- $\sigma_{\cot\theta} = 0.11$
- σ_z = 11 cm

SVT

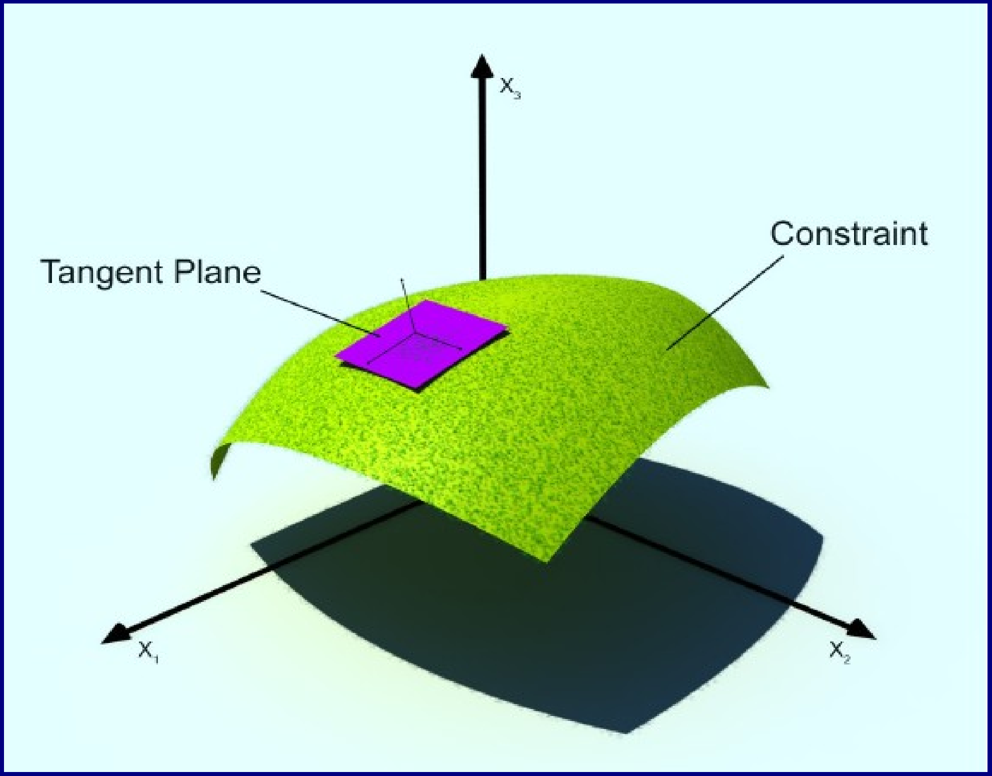
- eff ~ 90% (p_T > 2 GeV, d_0 < 1 mm)
- $\sigma_{d0} \sim 35\ \mu m$
- $\sigma_{pT} \sim 0.003\ p_T^2$
- $\sigma_\phi \sim$ 1 mrad

SVT – Track Fitter

Non linear geometrical constraint for a circle → F(x1, x2, ...) = 0



For small displacements → F(x1, x2, ...) ~ a0 + a1 Δx1 + a2 Δx2...
(ai = constant)

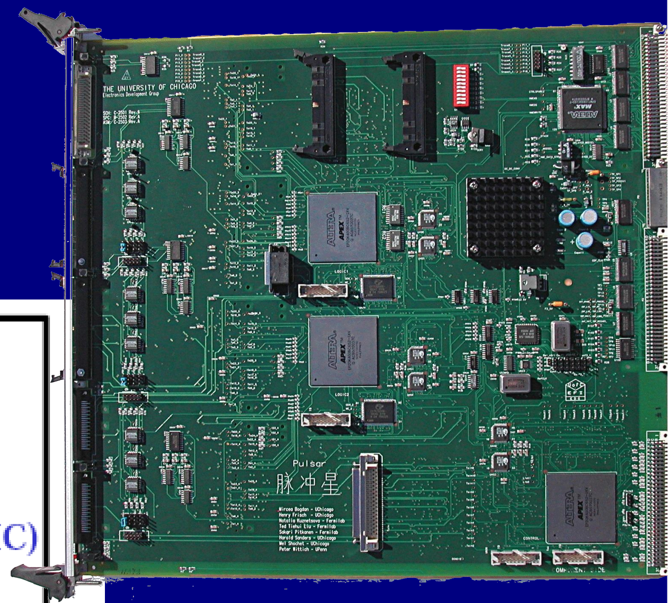


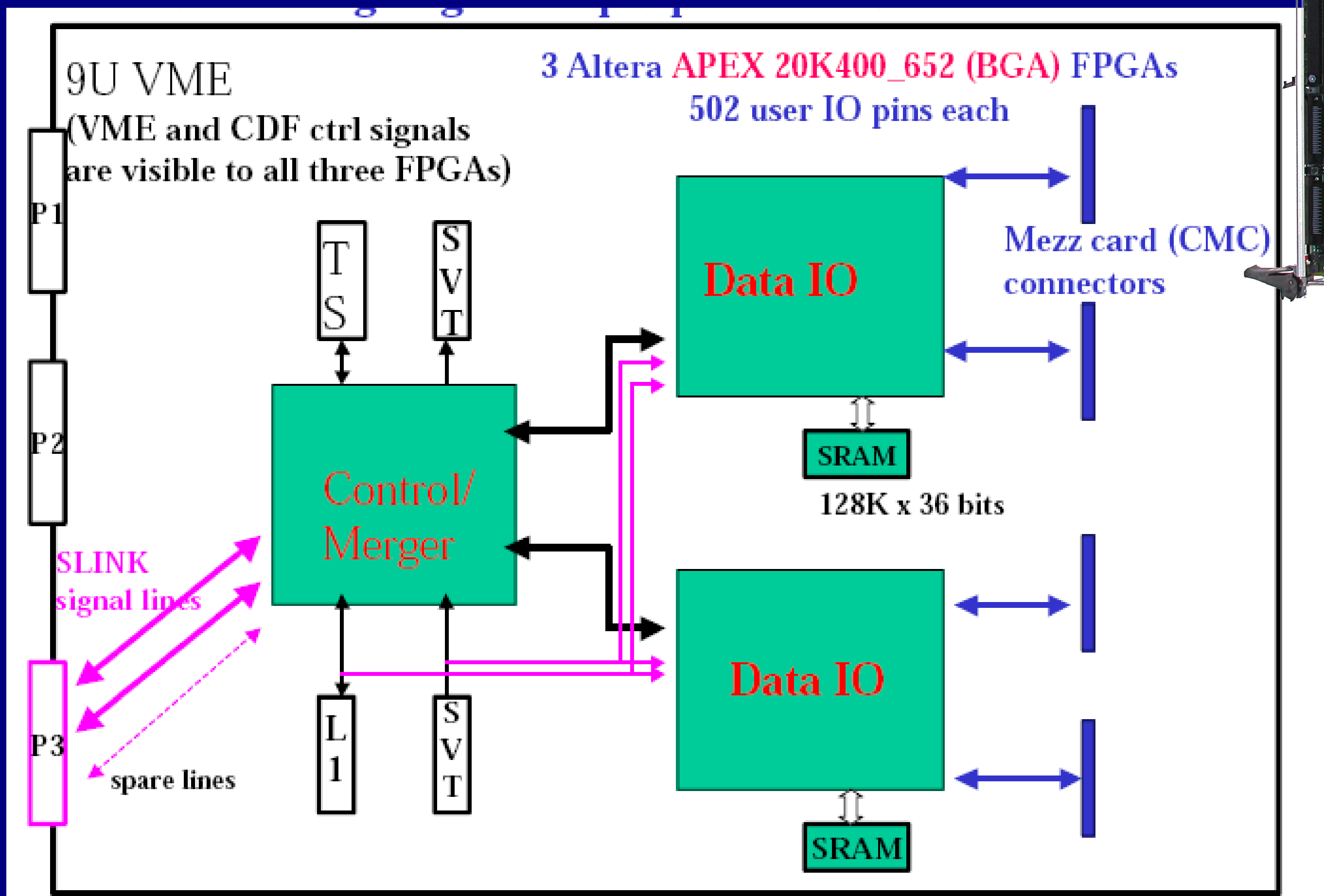
6 coordinates (4 SVX hits + Pt and Phi from XFT) – 3 parameters ti fit → 3 constraints that can be locally linearized

Track parameters → $p \sim c_0 + \Sigma_{i = 1,6}\, c_i x_i$

A single set on constants c_i is good for a whole detector wedge (30° in φ)

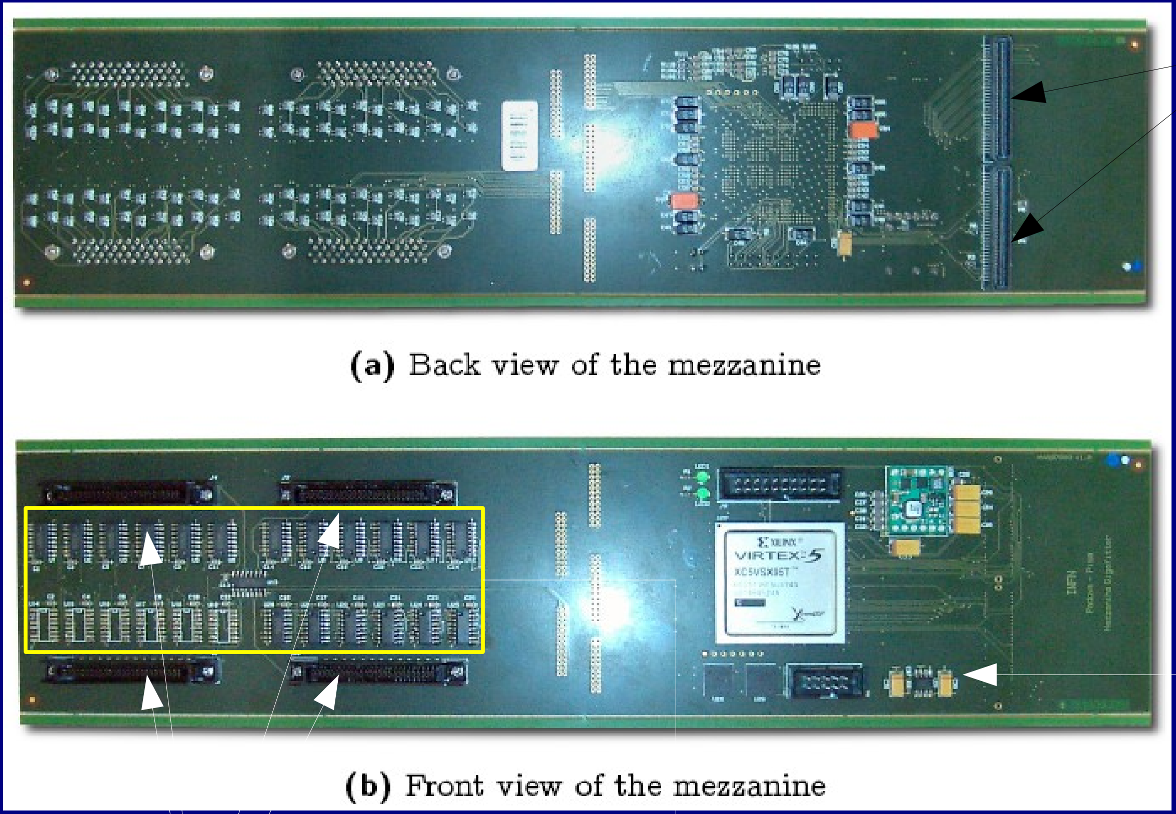
Pulsar Board





3 APEX20K400-1XV FPGAs on board = 3 Million system gates/80KB RAM per board
2 128K x 36 pipelined SRAMs with No Bus Latency: 1 MB SRAM (~5ns access time)

The GF Mezzanine


(a) Back view of the mezzanine

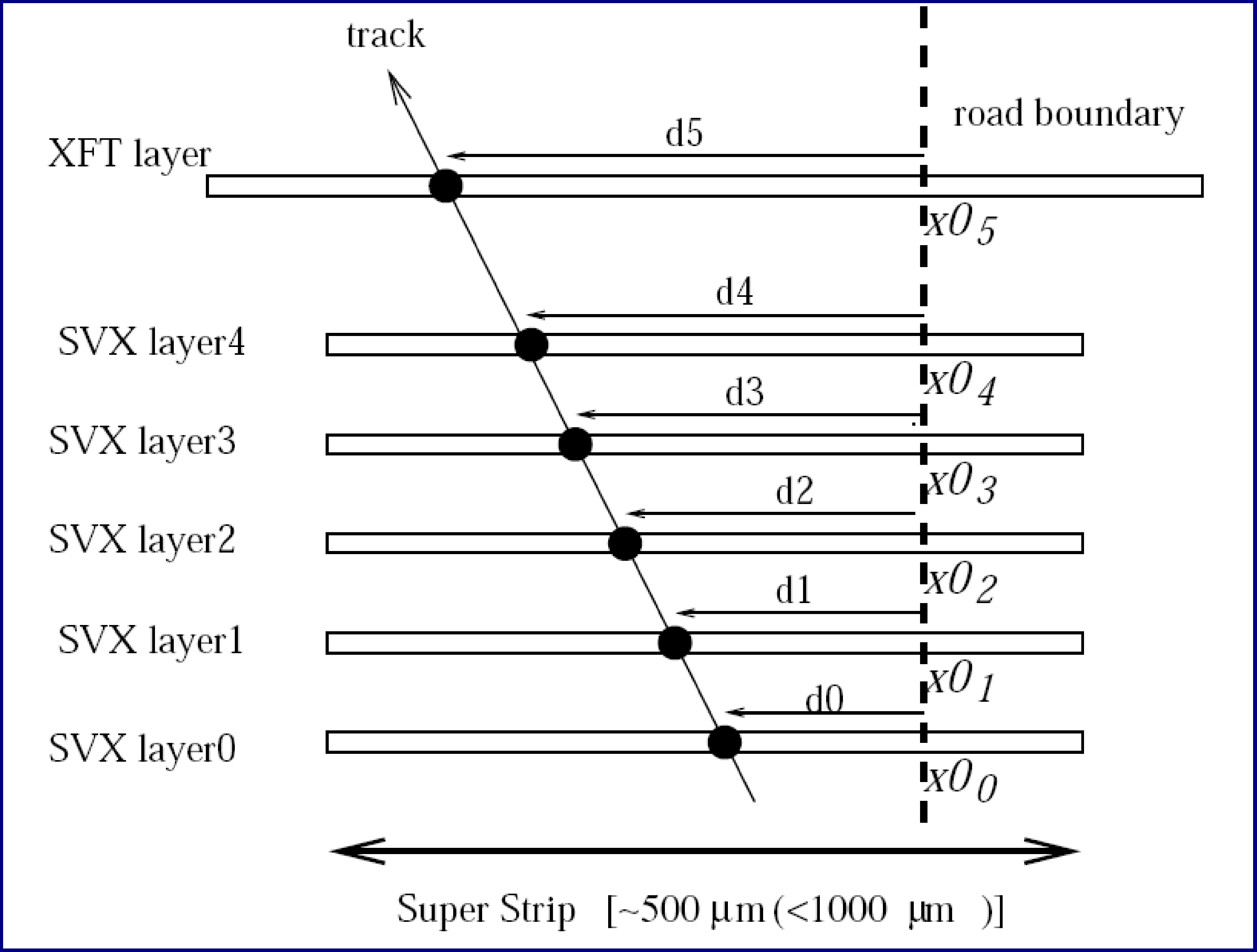
(b) Front view of the mezzanine

Interface with the Pulsar based on 2 64 pins PMC IEEE 1386 connectors

EEPROM to program the FPGA at every startup

Connectors (52 pins KEL_8830E-052-170S) to receive the SVX + XFT inputs

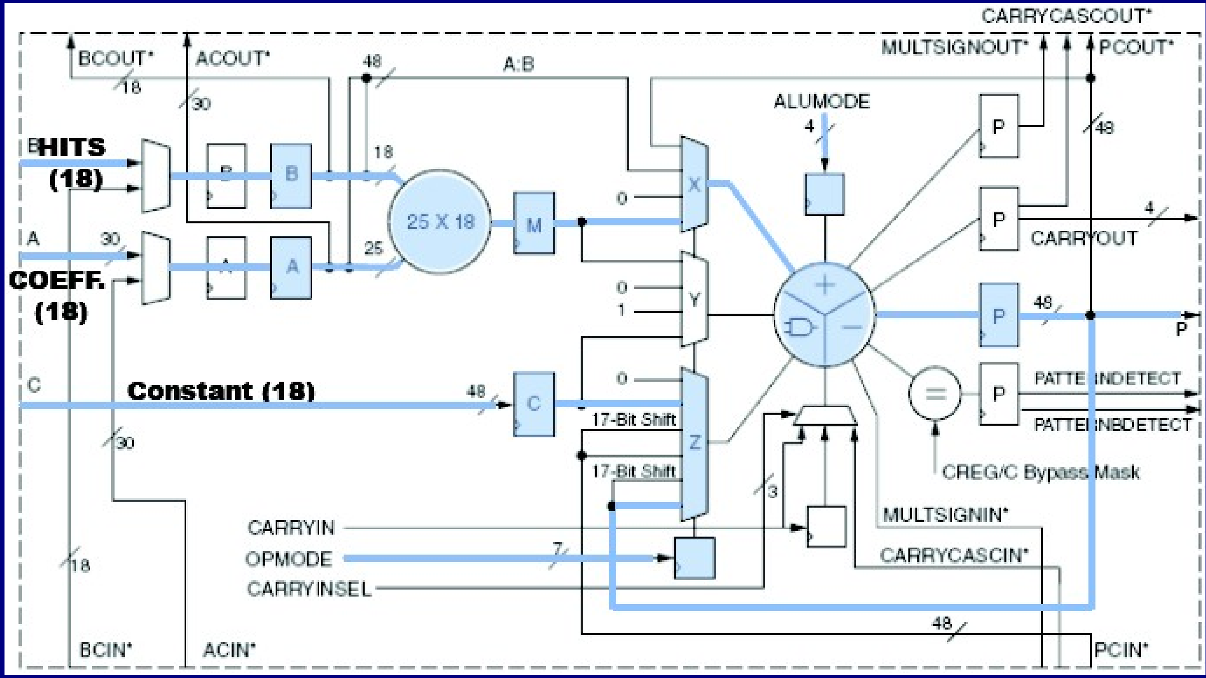
24 receivers and 1 driver to allow the translation from LVDS to TTL signals

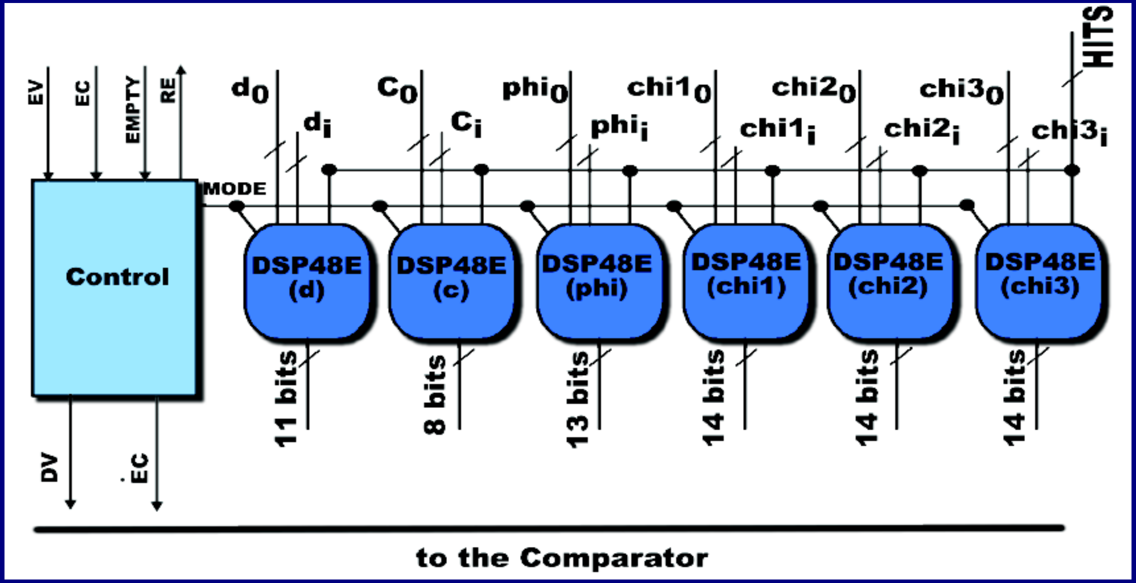

track
road boundary
XFT layer
d5
$x0_5$
d4
SVX layer4
$x0_4$
d3
SVX layer3
$x0_3$
d2
SVX layer2
$x0_2$
d1
SVX layer1
$x0_1$
d0
SVX layer0
$x0_0$
Super Strip [~500 μm (<1000 μm)]

The fitter

DSP inputs:
- **hits** (track coordinates x_i)
- **coefficients** (f_i and q_i)

DSP output:
- **fit parameters**





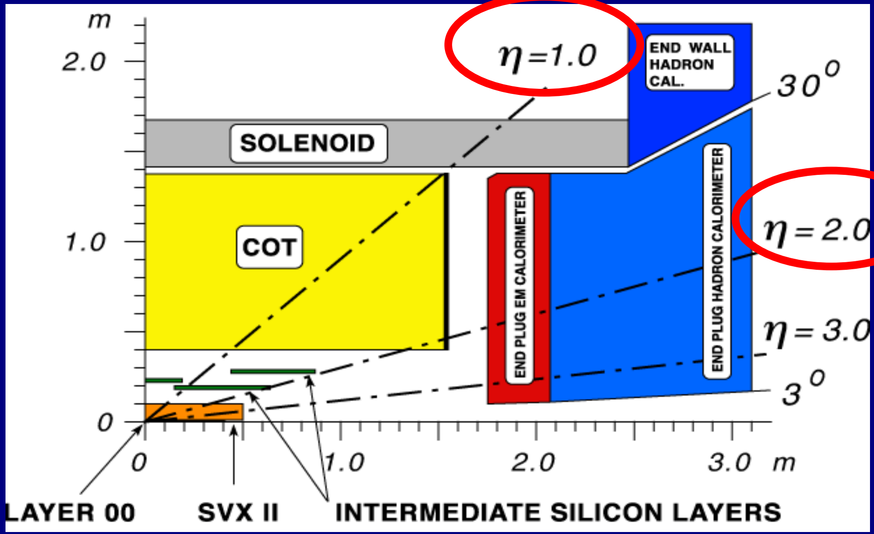
6 output parameters:
- impact param d0
- curvature c
- azimuthal angle Phi
- chi2_1, chi2_2, chi2_3

Where do we gain? - II

SVT Acceptance

Greater available memory
→ include patterns for

- silicon only tracks for a larger eta coverage



Useful to trigger on forward electrons, muons and taus.
Important to increase Higgs acceptance.

- extension of the acceptance in track p_T and impact parameter d

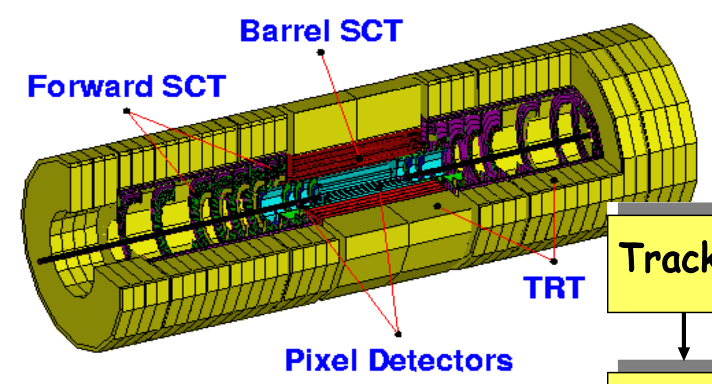
$p_T > 2$ GeV/c ⟶ $p_T > 1.5$ GeV/c

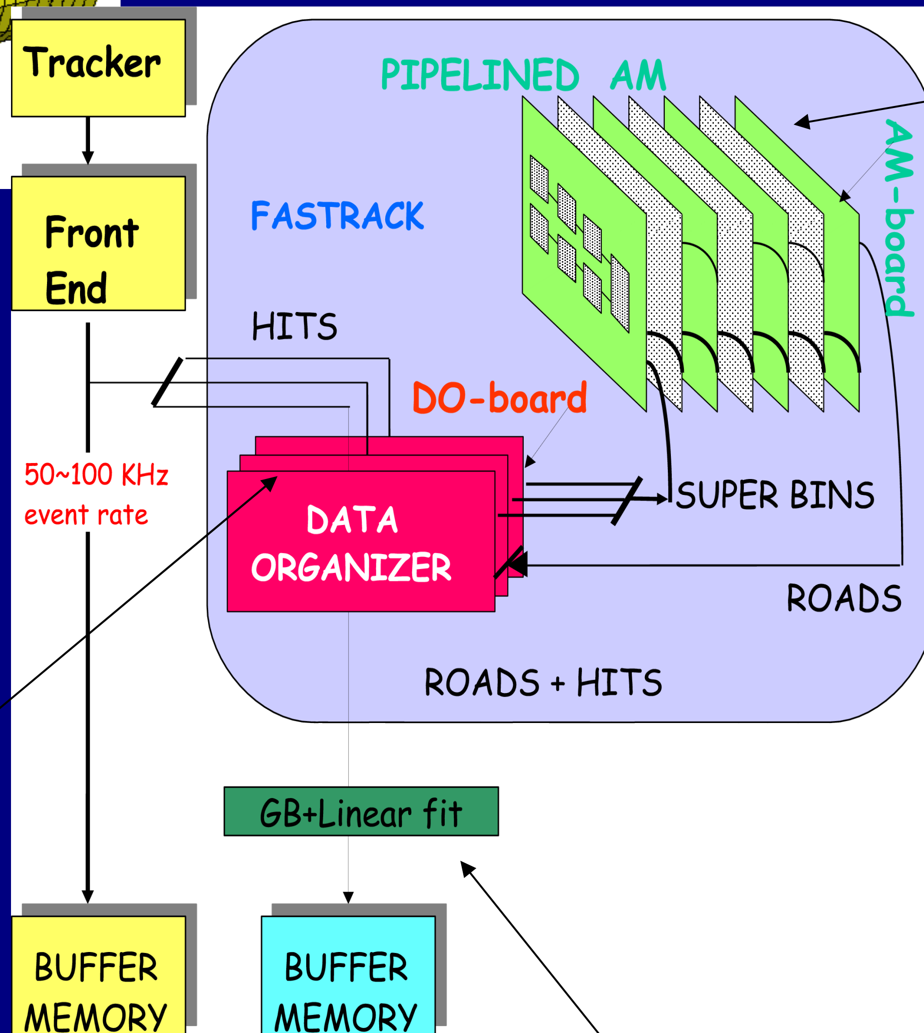
Improves lifetime measurements

d < 1.5 mm ⟶ d < 2-3 mm

Better b-tagging efficiency

FTK





- Performs pattern recognition on Super Bins
- Send back found roads to DO

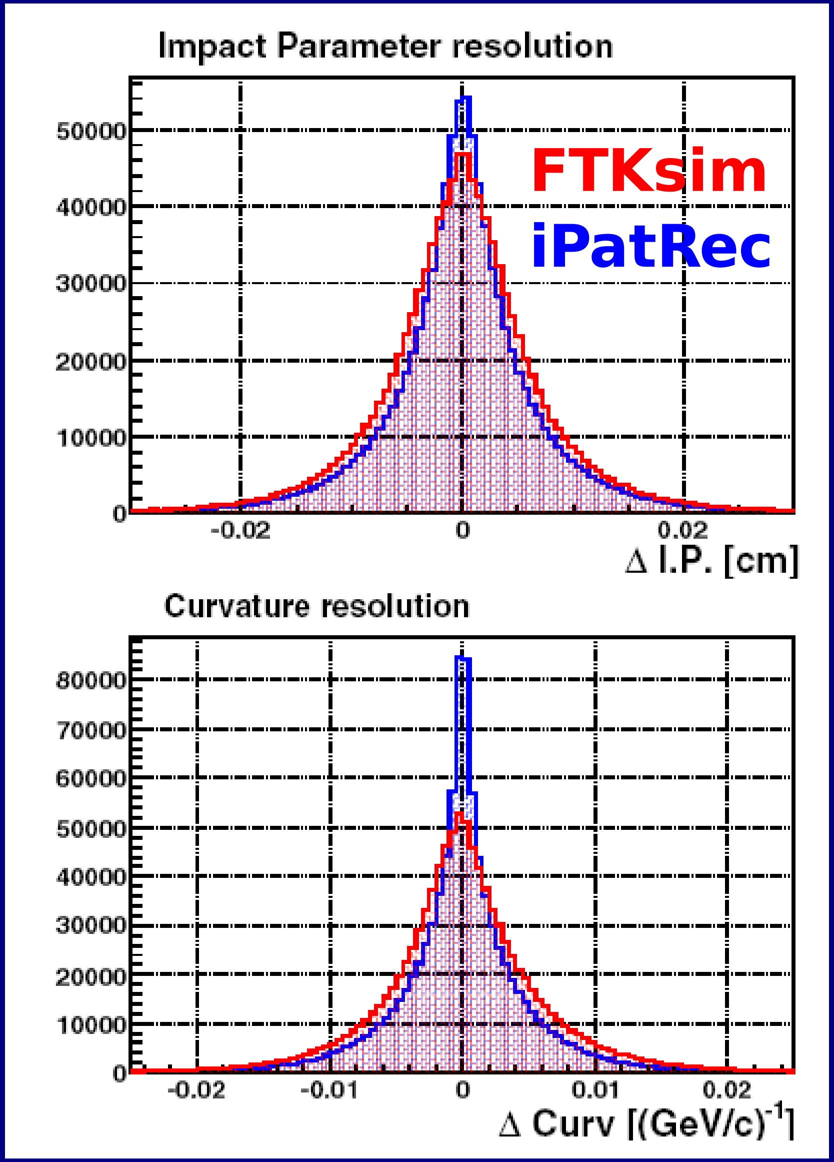
Current implementation of FTK uses all 11 silicon layers (4 R-ϕ + 4 stereo SCT layers and 3 Pixel layers)

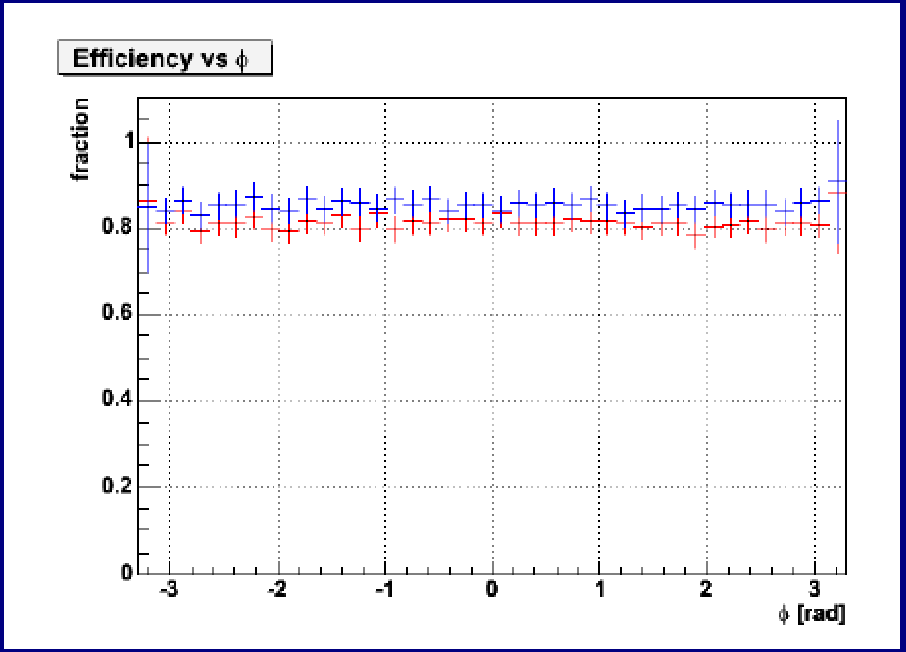
- Receives hits from DAQ
- Communicates with Associative Memory boards
- Sends hits & found roads to the Fitter
- 6 boards in parallel
- Each DO handles 1-2 layers

Roads and hits with high resolution are composed and the Linear Fits executed to select real tracks, stored in a buffer ready for the LVL2 CPUs

FTK tracking performances

Evaluated using FTKsim
Compared to the full online reconstruction program (iPatRec v10.0.6)





FTK - Charged tracks at Level 2

- Without FTK
  - Tracks are reconstructed only inside the RoIs
    - Difficult to substain high rates
  - LVL1 rates cannot be large since not enough powerful reduction is available at LVL2
    - LVL1 thresholds are high, physics losses
- With FTK
  - Tracks are reconstructed with high quality inside the whole ID
  - LVL2 strategies EARLY based on tracks produce stronger reductions than pure muon-calorimetric strategies
    - Lower LVL1 thresholds, physics gains.

b-tagging **τ-tagging**