

Gigafitter: performances at CDF and perspective for future applications

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Outline

- 1 Introduction
- 2 Gigafitter
- 3 Timing measurements
- 4 Future applications
- 5 Conclusions

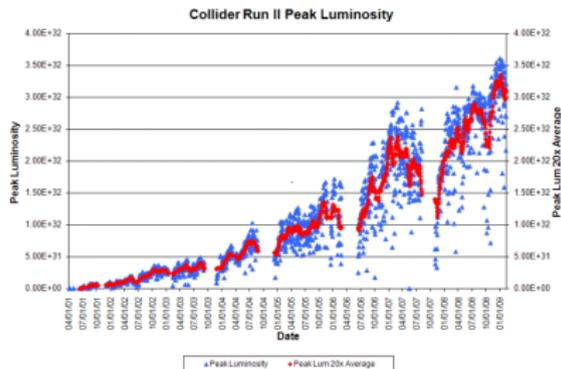
The GigaFitter is a next generation track fitter processor designed to upgrade current SVT TF++ processor at CDF experiment. The design could be used also to build more powerful track fitters for future experiments.

- 1 Introduction
 - CDF at Tevatron
 - SVT
 - SVT - TF++
- 2 Gigafitter
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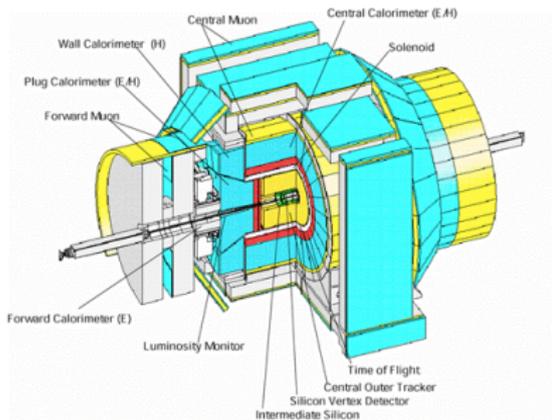
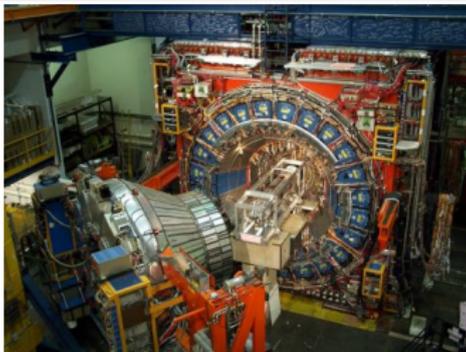


The Tevatron at Fermilab (Batavia, IL, USA):
proton-antiproton collider with
center of mass energy of 1.9 TeV
and $L > 3 * 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$
High rate of events.

Performance the accelerator
steadily increasing over time.

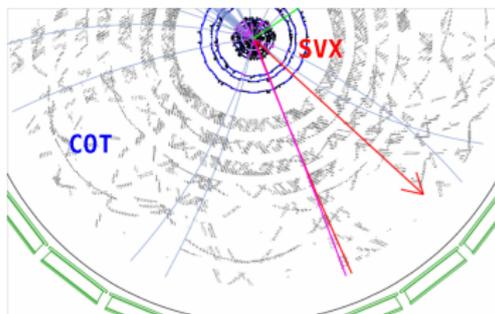


Trigger computing power must
evolve to reject the increasing
background.



Particle tracking:

- Powerful tool for online event selection



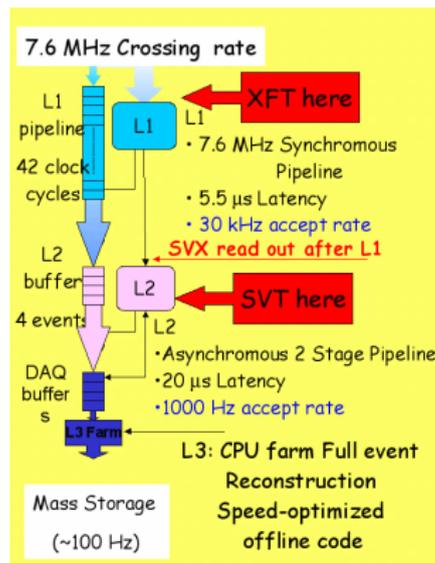
Tracking detectors: COT (multiwire drift chamber), SVX, ISL and L00 (silicon detectors).

XFT:

- COT tracks reconstruction
- $5.5 \mu\text{s}$ latency

SVT:

- SVX + XFT tracks reconstruction
- $20 \mu\text{s}$ latency
- Offline quality resolutions - impact parameter is reconstructed with $\sigma \approx 35 \mu\text{m}$
- Important element of both high precision B-physics and Higgs triggers

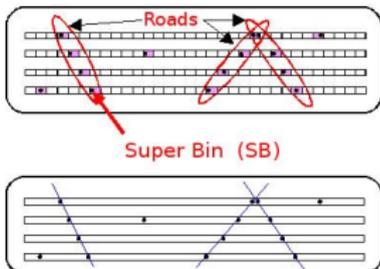


Online tracking is performed by XFT (level-1) and SVT (level-2).

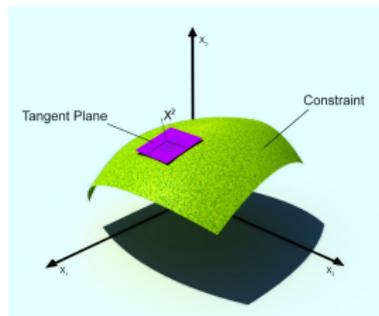
Silicon Vertex Trigger

Associative Memory

Linear Fit



Combinations inside a road.



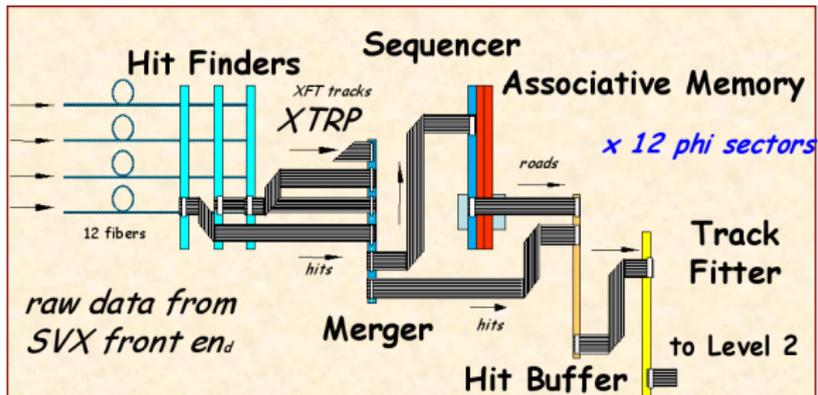
Fixed bank size:

- Large roads \rightarrow larger acceptance
- Small roads \rightarrow less combinatorial problem

Linearize problem: fits are scalar products

SVT hardware:

- ~100 9U VME boards
- 7 different kinds of boards
- one kind of cable for interconnections
- scalable and flexible design



- 16 VME boards (12 for processing + 4 merge data)
- 8x8 bit multiplications + precomputed terms of scalar products
- Fit only one of 5 combinations if 5/5 SVX hits are present
- Maximum 32 combinations per road fitted
- Precomputed terms scale with pattern bank → **limit to associative memory size**
- Cut with many combinations → **limit to road size**
- Not all possible fits done → **less efficiency**

A next generation track fitter may solve this issues!

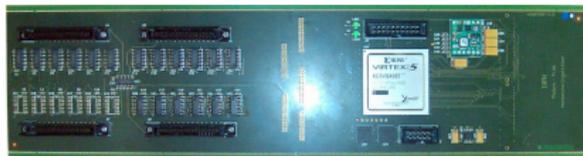
1 Introduction

2 Gigafitter

- Hardware
- Algorithm design
- Fit line
- Parallelism inside a fit line
- Further parallelism
- Debug and tuning features

3 Timing measurements

4 Future applications



- 3 GF mezzanine on Pulsar motherboard
- GF mezzanine receive up to 4 data streams
- One single system can process **all 12 SVX wedges**
- Capable of all possible fits

Xilinx Virtex-5 VSX.

Thanks to Xilinx for kind donation.



640 DSP:

- 25x18 bit multipliers
- 48 bit adders

Full resolution linear fit scalar products.

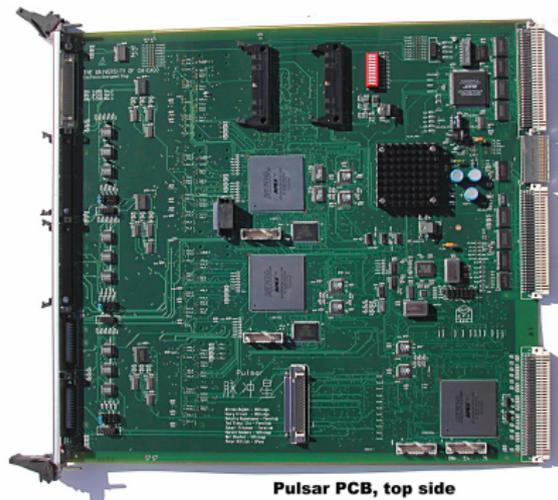
Pulsar

Flexible 9U VME board:

- Three FPGA processors
- 4 mezzanine expansion slots
- Many connectors (including IN and OUT SVT type)

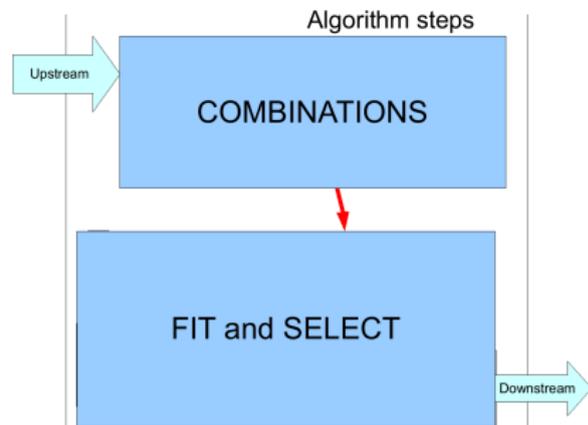
In CDF used by L2 Global and SVT.

Used also outside of CDF: Magic.



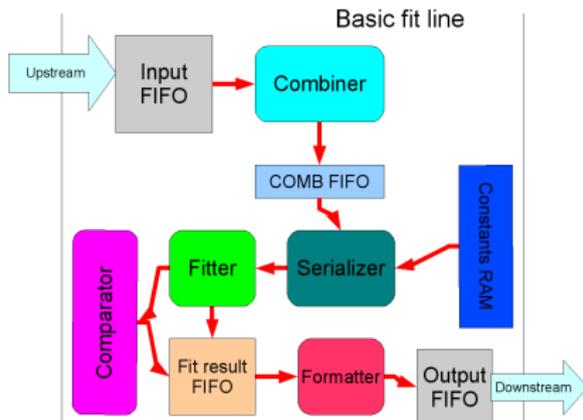
The algorithm of a single fit line can be subdivided in two pipelined steps:

- Receive hits from a road found in the AM. Compute all combinations of hits.
- Fit all combinations, cut on χ^2 , select the best fit among several good.



Basic structure of the algorithm.

- Combiner - receive hits and produce combinations
- RAM - fit constants, several sets: layer/barrel/long cluster selection
- Serializer - serialize hits+constants for Fitter
- Fitter - perform the scalar products
- Comparator - compute χ^2 then quality cuts; compare with previous fit
- Formatter - fetch accepted tracks and send downstream

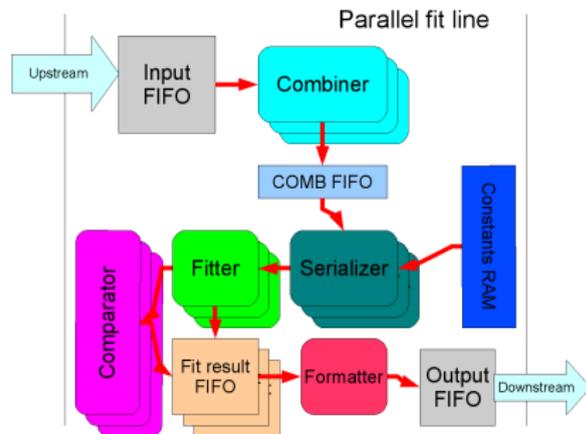


7 DSP used.

1 fit every 6 clock cycles.

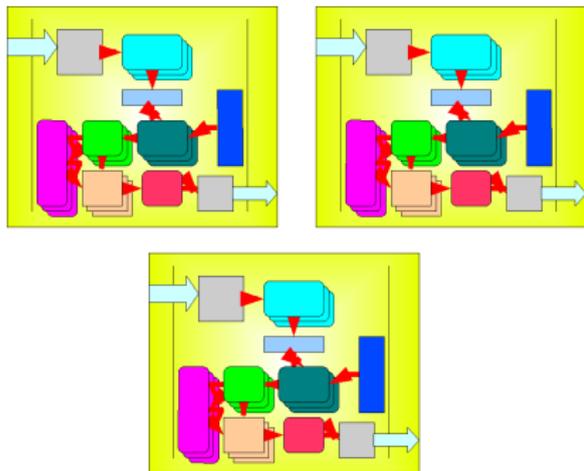
Parallelism possible in both pipelined stages:

- 2-3 parallel Combiners to eliminate deadtime (when a Combiner is writing, another is reading and viceversa)
- 6 parallel Fitters+Comparators to maximize fit output rate



42 DSP used.

1 fit every clock cycle.



Up to 3 fit lines on the same wedge.

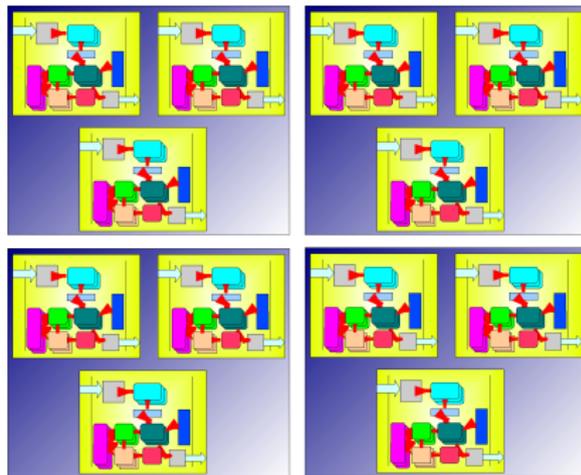
126 DSP used.

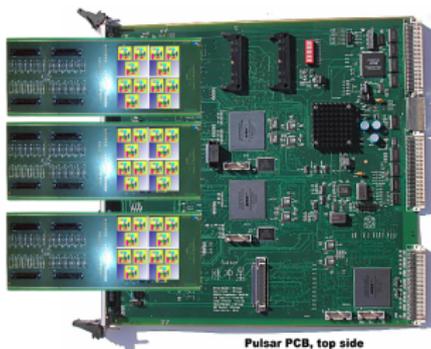
3 fit every clock cycle.

4 independent fit blocks, one each input.

504 DSP used.

Up to 12 fit every clock cycle.



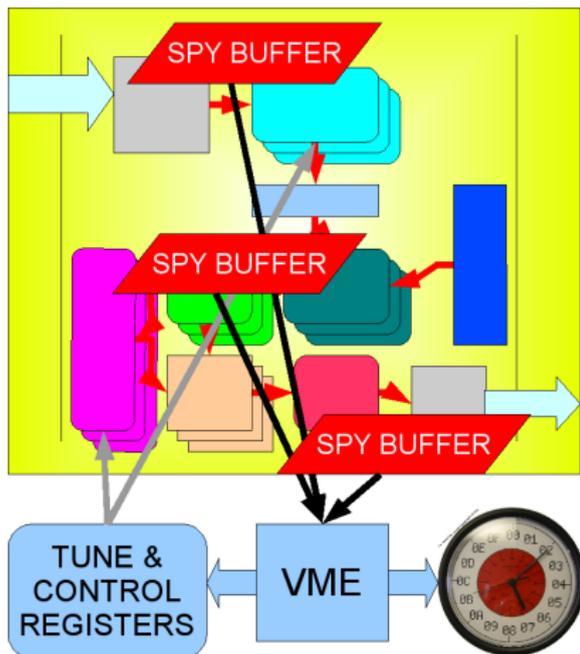


Final system has 3 parallel GF processors.

Up to **36 fit every clock cycle**.

At an internal clock of 100 MHz (tested w/o optimization on a single fit line): **3 fit every ns**.

- Higher clocks possible on FPGA (limited at 550 MHz for DSP and BlockRAMs), but we are limited by power consumption.
- It's possible a balance between resources (less parallelism) and internal clock.
- Modular design allow us to explore different solutions.



Advanced debug features:

Spy buffers

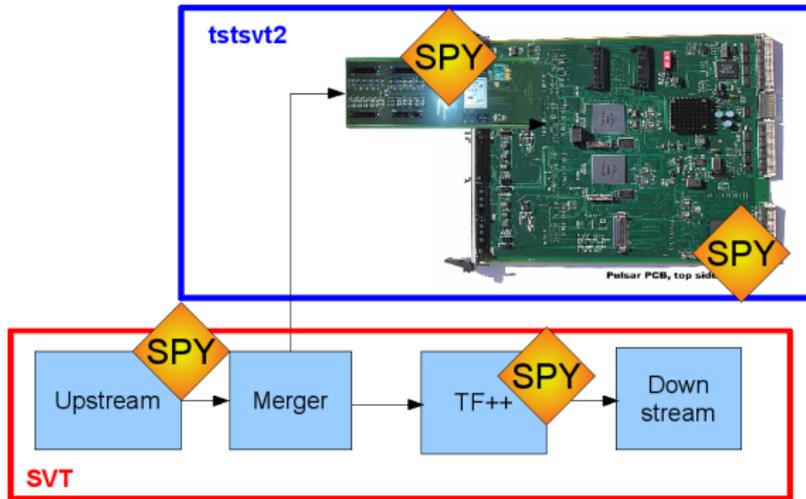
- Circular memories spying data flux
- Freeze and read by VME at any time
- Used to compare input → output of GF and simulation
- **Online monitoring**

Clock and regs:

- Computing clock frequency can be adjusted via VME
- Control registers for tuning fit line (χ^2 cut, ...)

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 - SVT + GF in parasitic mode
 - GF vs TF++
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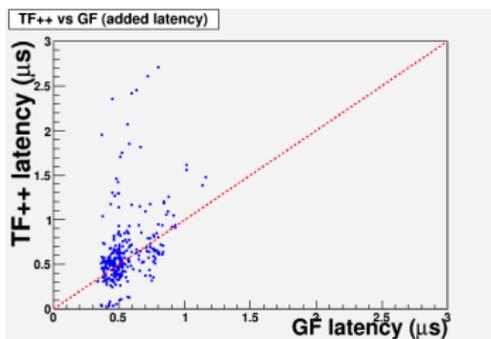
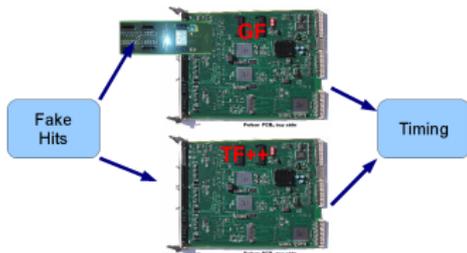
GF can be run parallel to SVT, no interference with normal CDF running



Reading Spy Buffers we can snapshot input/outputs of both GF and TF++, simulate and compare.

Fast development during data taking.

- GF with one fit line w/o parallelism (1 fit every 6 clock cycles @ 120 MHz)
- Fake hits sent thru SVT
- HitBuffer output split and sent to both TF++ and GF
- Time of End Event in input and output by both systems recorded



- Latency added by both boards measured
- GF has a fixed minimum latency of $\sim 400\text{ns}$
- TF++ latency can go up if event is complex
- GF is fast enough to limit latency for all kind of events

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- GF type track fitter can be used in **future online tracking processors**
- **FTK** is a proposal for an SVT-like tracking at ATLAS level 2 trigger, GF can be used in early phase of FTK and expanded to be the track fitting part of the processor
- **GF modular desing** scale easily with suitable hardware



- Boards such as **Janus supercomputer** can be used as a base for a future track fitter for LHC
- Janus is made with 16 FPGA on small mezzanines in a single 9U board

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 - Scalable to bigger/faster hw → **track fit for future experiments** (ie. LHC)

Backup slides

6 coordinates: $x_1, x_2, x_3, x_4, x_5 (P_T), x_6 (\phi)$

3 parameters to fit: P_T, ϕ, d

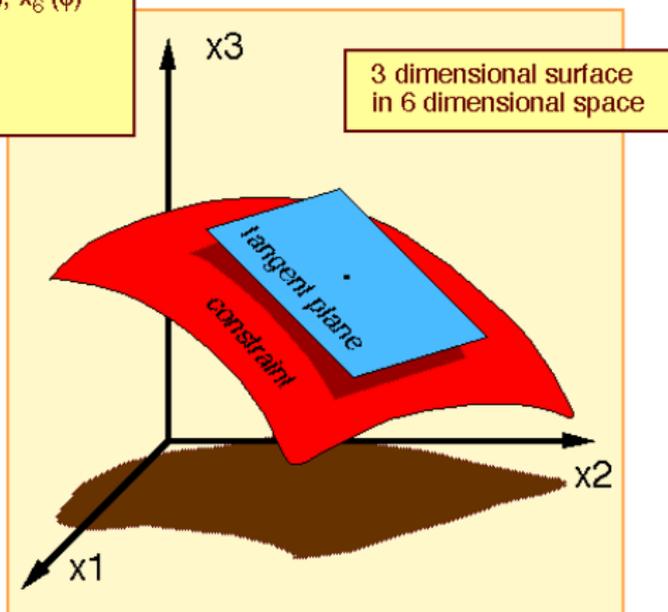
3 constraints

tangent plane:

$$\sum_1^6 a_i x_i = b$$

track parameters:

$$d \approx c_0 + \sum_1^6 c_i x_i$$



Linear approximation is so good that a single set of constants is sufficient for a whole detector wedge (30° in ϕ)