

Justification for modifying FTMs

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Introduction

The CDF Silicon detector because of the way it was designed and installed cannot be reached for maintenance on its delicate internal parts that are inside the CDF tracking volume. Systematic unrecoverable failure modes on these parts have been associated to particular running conditions with high occupancy and/or high dead-time. It is the first priority in the Silicon Group to prolong as much as possible the lifetime of the CDF silicon detector. As a consequence any means that can prevent/mitigate these failures should be implemented as soon as possible.

Motivations for the modification

It has been proven that wire-bonds can break due to fatigue stress accumulated at the heel and induced by resonant motions¹.

Out of 12 failures so far accumulated 11 has been correlated with running condition where chips in the silicon modules (ladders) were driven to a mode with high occupancy.

This mode of operation can be triggered by either:

1. sending a 5th L1A to the readout chips (they have a 4 deep buffer)
2. Missing a PRD2 (this command erase a L1A) and so still ending up overflowing the 4 deep buffer)
3. Missing a FECLK cycle (132 nsec period clock). If this happen when the PRD2 command is issued the command is not effective and we get back to overflowing the 4 deep buffer.

The first approach to minimize the impact of such mode of operation was to spot it with the online consumer SVXMON and trigger a request for a hard reset of the hardware.

This is a successful way to minimize the time during which the modules run in the dangerous mode.

An investigation started to try to eliminate the source of the mode. The 3 points mentioned above are strongly correlated with the reliability of the differential transmission line that drives the chips in the CDF Silicon Detector. The drivers² for this transmission line are mounted on the FTMs³ (FIB Transition Module) that are installed in the VME crates located in the CDF collision hall.

The output power of these drivers is settable by resistors and jumpers in the FTMs.

The online consumer SVXMON has been used to select the boards that go in the dangerous mode more often than other. Nine FTMs selected this way have been modified according to the section that follows. So far the rate of success is 100 %. The dangerous mode did not yet show up on the modified boards after up to 7 weeks of integrated running time.

The Silicon Group is still prioritizing the list of boards that will be modified according to the failure rate during data taking. The decision to modify every single board has been

¹ <http://www-cdf.fnal.gov/upgrades/silicon/TASK-Force/report-11-27-02.PDF>

² http://www-ese.fnal.gov/eseproj/svx/ten_bits/pdrv_rev2v.pdf

³ http://www-ese.fnal.gov/eseproj/svx/svx3_fib/fibspc.pdf

already taken. We are now modifying boards one or two at the time during short accesses and we are evaluating the possibility to ask for a long access (approximately 3-4 days) to implement the modification to all the FTM boards in the system.

As a byproduct of the resets induced by the appearance of the dangerous mode the CDF experiment is experiencing an additional down-time in the few % level due to the frequent resets. Furthermore the dangerous mode is accompanied by high occupancy and so has a negative impact on the L1 and L2 trigger dead time.

What is the Modification and how long does it take to do the work.

The modification of the FTM board is simple but time consuming. It is a four steps operation.

1. Unplug the FIB timing cables (2) and the fibers (10) from the FTM board and removal of the FTM board from the VME crate. (Time needed 10 minutes)
2. Modify the FTM board according to the drawing in figure 1. Three resistors have to be replaced (from 33 K Ω to 5 K Ω) and 3 jumpers have to be added.(Time needed 15 minutes)

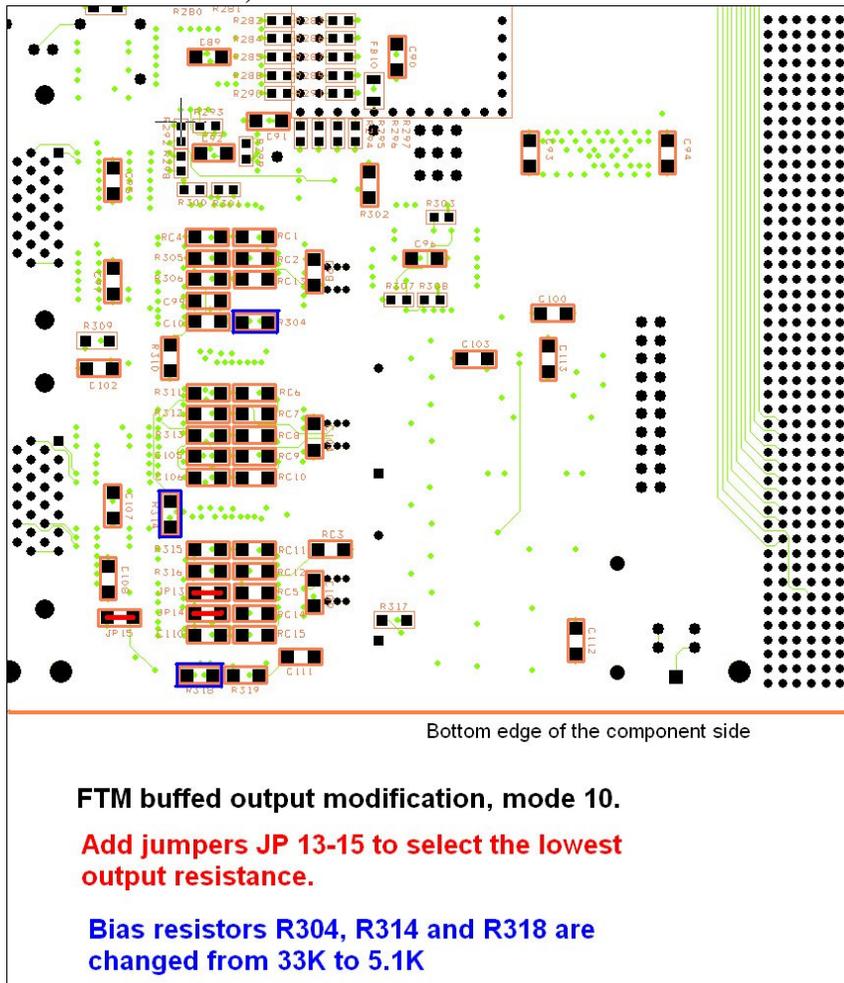


Figure 1: schematic of the FTM board with in BLUE the resistors to be replaced and in RED the JUMPERS to be inserted.

3. Re-installation of the FTM in the VME crate, re-plugging of the FIB timing cables, cleaning and greasing of the optical connectors and re-plugging of the fibers (Time needed 15-20 minutes)
4. Post modification functionality test. (Time needed 10 minutes)

The tools are now in place (and a JHA as well) to perform the work in the collision hall. This work can be pipelined up to a throughput of 1 board every 30 minutes. The impact on the signals quality can be seen in Figure 2.

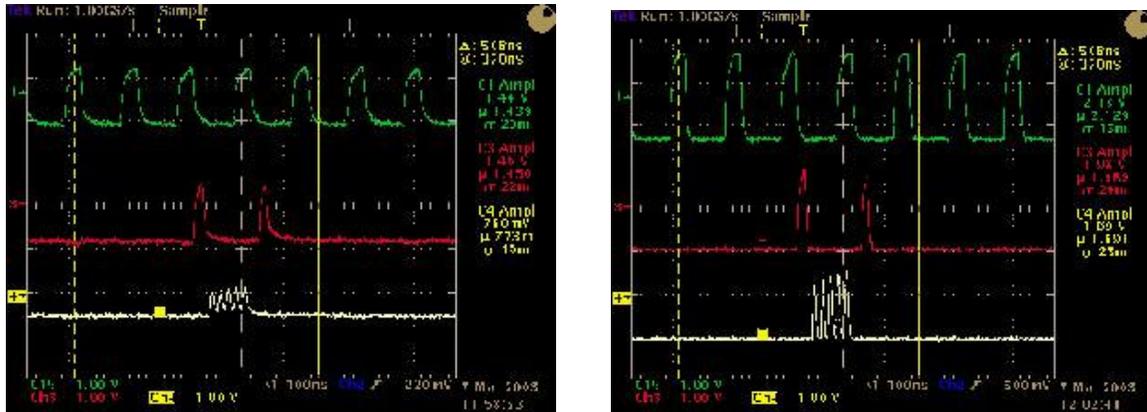


Figure 2: LEFT, differential signals as produced by a *regular* FTM, RIGHT differential signals as produced by a *buffered* FTM.

Boards Count

There are a total of 58 FTM boards in the CDF silicon detector. 36 of them are connected to SVXII ladders while 22 serve ISL and L00 modules. The SVXII ladders are of higher priority due to the fact that this sub-detector is the only one used for the CDF trigger and also because the design of the modules is more prone to the failure mode described above. 9 FTM boards have been already modified at this time. The boards are installed in 8 different VME crates 4 for SVXII and 4 for ISL/L00. The best estimate is that a SVXII crate will be completely finished within a shift of 8 hours. An ISL/L00 crate, due to the lower population of boards can be finished in a 6 hours period.

Conclusions and possible approaches

In order to prolong as much as possible the lifetime of the detector The CDF silicon Group has to minimize the time spent in the dangerous mode and so the accumulated stress due to fatigue on the wire-bond heels. The major possible source left of the dangerous mode has been identified to be on the driver of the FTM board and a solution is being implemented with a 100 % rate of success. This modification should be applied to all the boards in the system as soon as possible.

1. The most efficient way to accomplish the job would be a 4 days access.
2. As an alternative we could keep going with the approach of modifying the boards one by one prioritizing them according to the error rates. This second approach

would require frequent short (1-2 hours) accesses between stores. These accesses will be requested during the store according to the error rates observed during data taking. This does not imply that there will be an access request per store. A threshold of an error per hour is considered appropriate for the call. The CDF Silicon Group has the personnel and the equipment necessary to accomplish the job with the maximum efficiency. A list of trained people with a pager number will accompany every access request. A 24/7 coverage will be established so that we can take advantage of any access longer than 4 hours to finish a VME crate independently from the error rate.

This task is at the top of the CDF Silicon Group priority list.