L2 Decision Studies with PULSAR/PC

Kristian Hahn
University of Pennsylvania
10/10/03

Penn Participation

Kristian Hahn

Paul Keener

Joe Kroll

Chris Neu

Fritz Stabenau

Rick van Berg

Peter Wittich

Overview

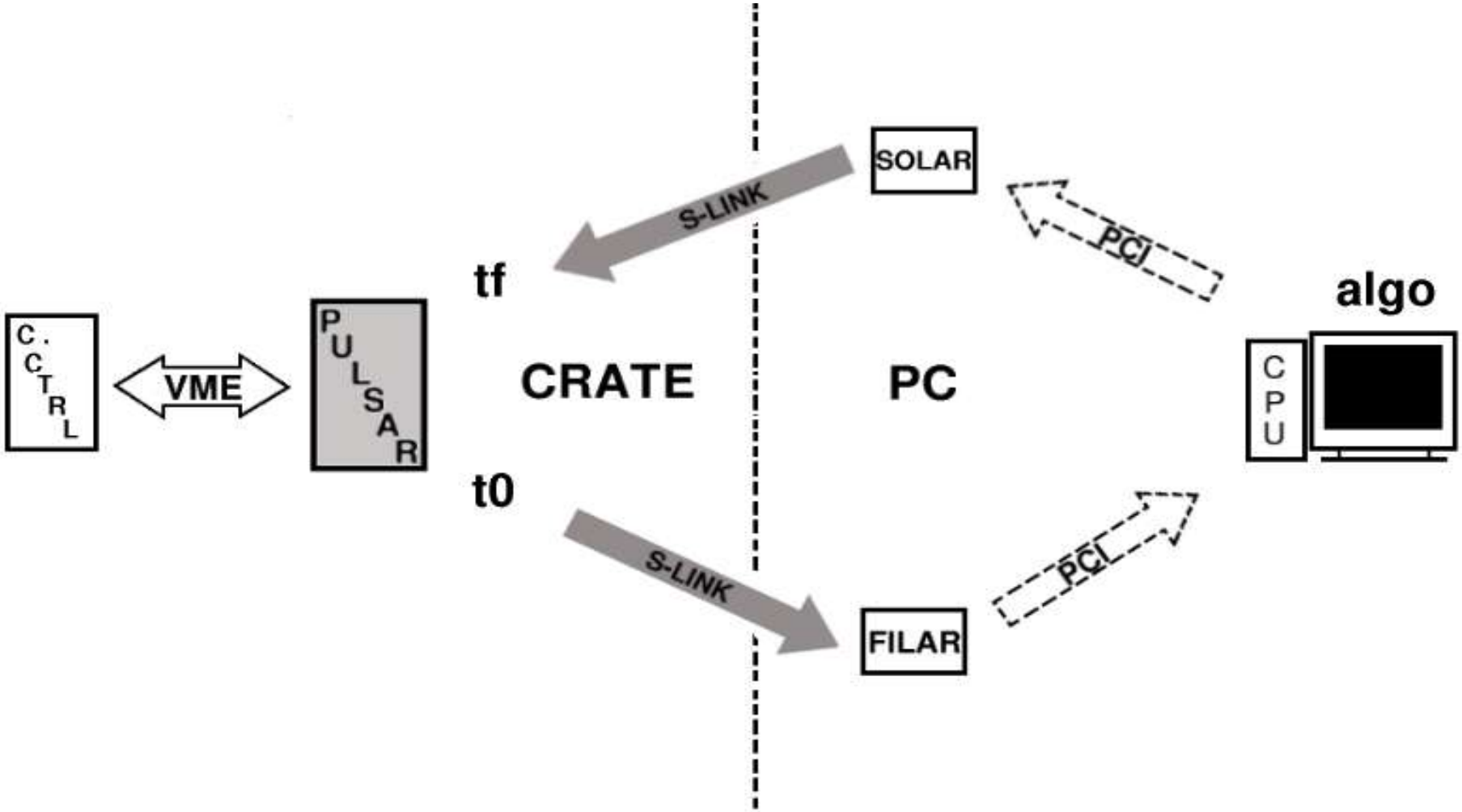
- The motive for E4:
  - Establish the PULSAR/PC scenario.
- Measurement Goals
  - Measure the time for the L2 decision process with a realistic experimental setup.
  - Understand and minimize the times associated with segments of the decision process.
  - Ensure the integrity of the returned L2 decision.

Experimental Setup

Our setup has evolved ...

- First: single PC
  - Stand-alone algorithm timing with TL2D data.
  - Measurements of limited scope.
- Then: PC ↔ PC
  - Round-trip timing of L2 decision process w/ S-Link.
  - Transition to S-Link formatted data.
  - Routing data over PCI bus on source PC unnecessary, adds latency.
- Now: PULSAR ↔ PC
  - Round-trip timing with a realistic hardware setup.
  - Zero suppressed, S-Link formatted data.
  - Firmware support for timing & L2 decision verification (Tomi).
  - On-board timing reduces measurement ambiguity.

Nice Graphic of Our Setup



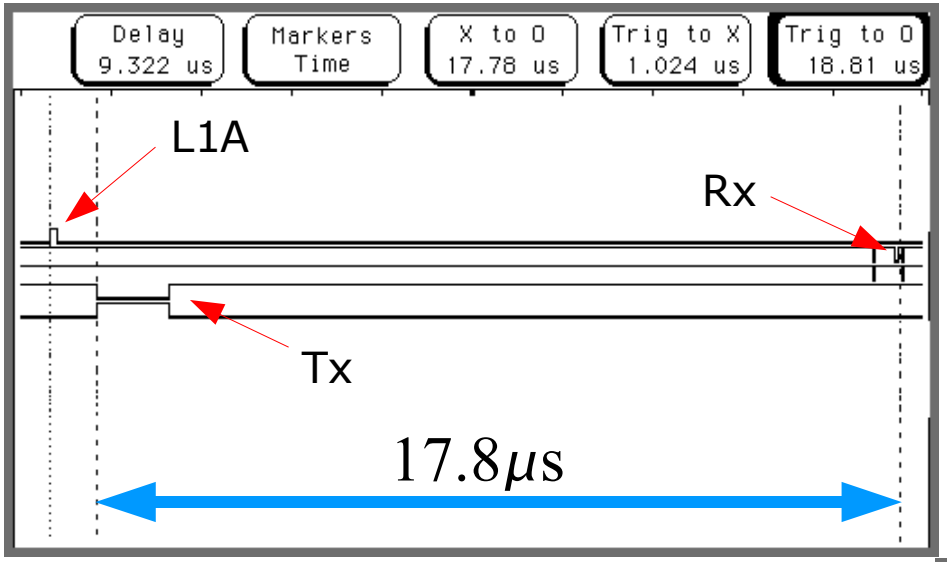
Round-Trip: Data Flow

- From the crate:
  - Use vxworks to initiate data transmission from the PULSAR.
    - Write the event data to a PULSAR RAM.
    - Send data with fake L1A, start timing (t_0).
- To the PC:
  - Receive data (s32pci64-filar).
  - Run algorithms, generate a L2 decision bit-mask.
  - Transmit bit-mask (s32pci64-solar).
- Back to the crate:
  - Decision bit-mask is written to a fifo on the PULSAR, stop timing (t_f).
  - FIFO readout with vxworks code.
  - Decision verified against the correct bit-mask from TL2D.

Round-Trip : Timing

- First approach: timing with vxworks
  - Start: after L1A call. Stop: Rx FIFO indicates it's "ready". ✘
  - Method includes VME communication with Controller (~5μs/call).
- Second approach: timing with a logic analyzer
  - Start: TX data strobe, Stop: RX data strobe. ✘
  - Per-event timing information not accessible.
  - Difficult to define the correct trigger condition for timing.
- Best approach: timing with PULSAR
  - Start: TX data strobe, Stop: RX control strobe. ✔
  - On-board counter /w VME readout → Per-event timing information.
  - Improved triggering → accurate round-trip timing.

Round-Trip : Timing Details (1 event)



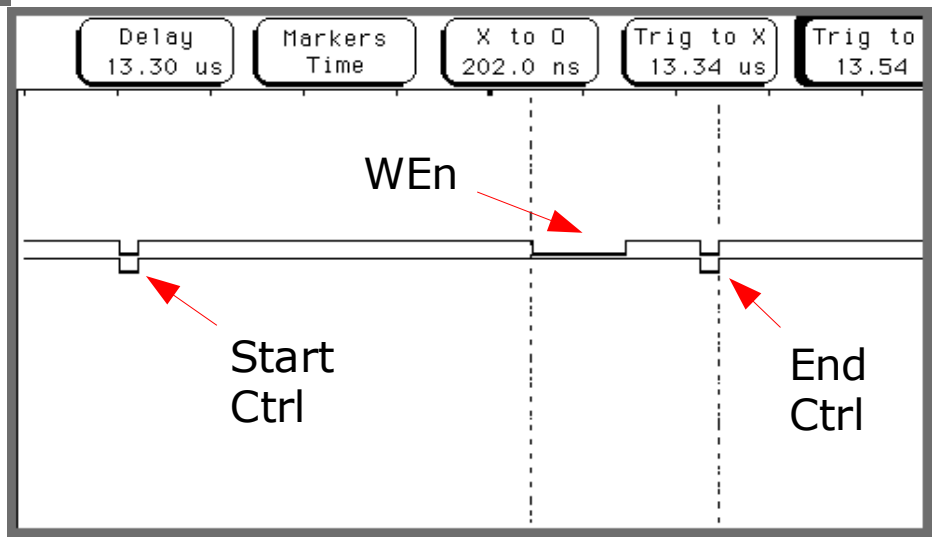
⇦ Roundtrip timing

Timing under 20μs !

(w/ algorithms!!)

Close-up of Rx signals ⇨

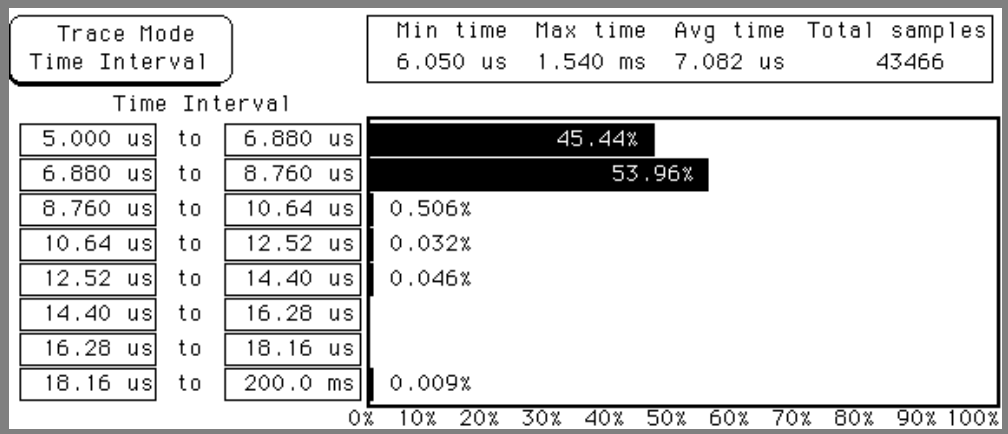
- Triggering on data WEn skews measurements ~ -0.2μs
- 0.6μs in delays. Firmware?

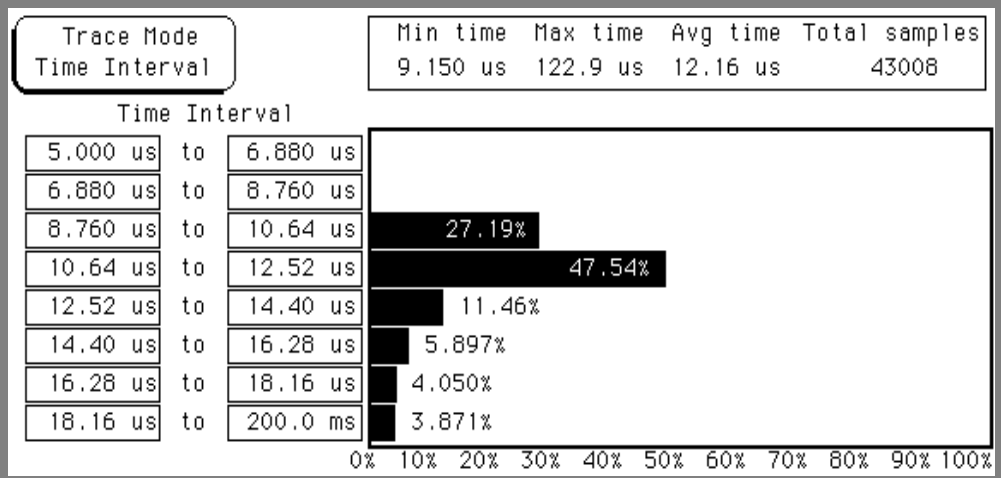


Round-Trip : Plots (analyzer)

1.8 us bins, last bin to 200ms

63k events, ZS 1_04-v2 data



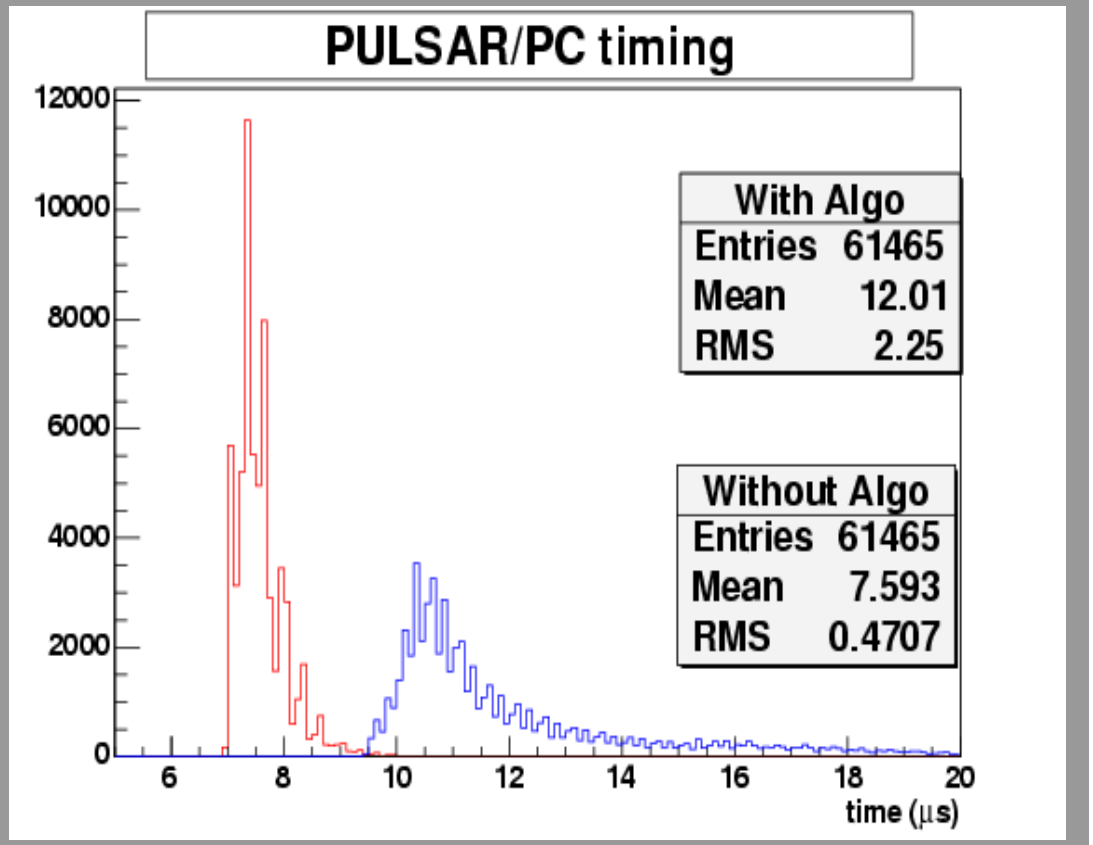


- Without algorithms
  - 7.1 μs mean
  - Negligible occupancy for 18+ μs bin
- With algorithms
  - 12.2 μs mean
  - Max time = confusing
    - Analyzer artifact?

Round-Trip : Plots (PULSAR)

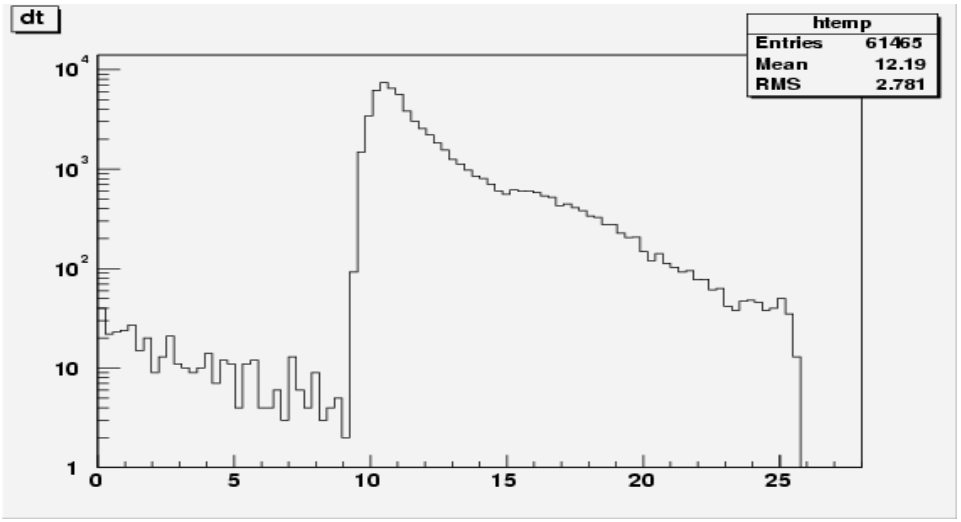
w/ algo : Blue w/o algos : Red

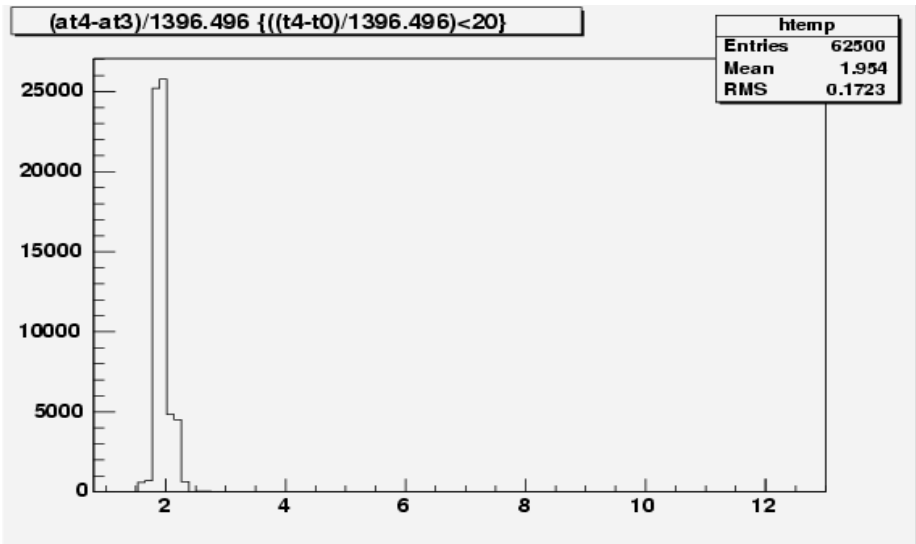
0.1 μs binning, 63k evts ZS 1_04v2



- Consistent
  - Means: 12.0μs ,7.6μs
    - Analyzer: 12.2μs, 7.1μs
    - PC↔PC : 16.3μs, 12.7μs
- I/O bound (in the peak)
- Algorithmic tails

Round-Trip : Timing Features





- Counter wrapping
  - Effects only the PULSAR plots.
  - 10 bit count = 25.8 μs max.

- 4 μs btw off. algo/no-algo
  - w/ PC-PC, 2μs
  - Repeated object instantiation
    - Will remove!

Round-Trip : Time Accounting

1. Start timing overhead
2. Getting data to S-Link connector
3. S-Link connector to S-Link fibre
4. S-Link fibre
5. S-Link fibre to S-Link connector
6. S-Link connector to S32PCI64 buffer
7. S32PCI64 buffer to memory
8. memory to unpacking
9. Algorithms
10. memory to S32PCI64 buffer
11. S32PCI64 buffer to S-Link connector
12. S-Link connector to S-Link fibre
13. S-Link fibre
14. S-Link fibre to S-Link connector
15. Data transfer inside PULSAR
16. Stop timing overhead

Work in Progress

L2 Decision Integrity

- Decisions generated on the PC are correct (63K evt).
- 0.01% discrepancy seen on the PULSAR.
  - Missing EOF from a bitmask packet appears in the next.
  - Same issue & rate seen in a l0M event study.
    - Solar?
    - PULSAR firmware?

Conclusions & Directions

- Further evidence that we're I/O bound!
- PULSAR/PC timing looks good! (better than “promising”)
- From here ...
  - Optimizations
    - New filar/solar firmware may improve timing.
    - Direct unpacking of S-Link formatted into data structures.
    - Repeated Trigger Object Instantiation removal.
  - Documentation
    - CDFnote in the works.