

# PC Tests with SVT Latency

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# Overview

- Constraint:
  - SVT data arrives  $\sim 20-80\mu s$  after L1A
- Response:
  - separate S-LINK's for SVT/non-SVT data
  - start non-SVT triggers without waiting for SVT

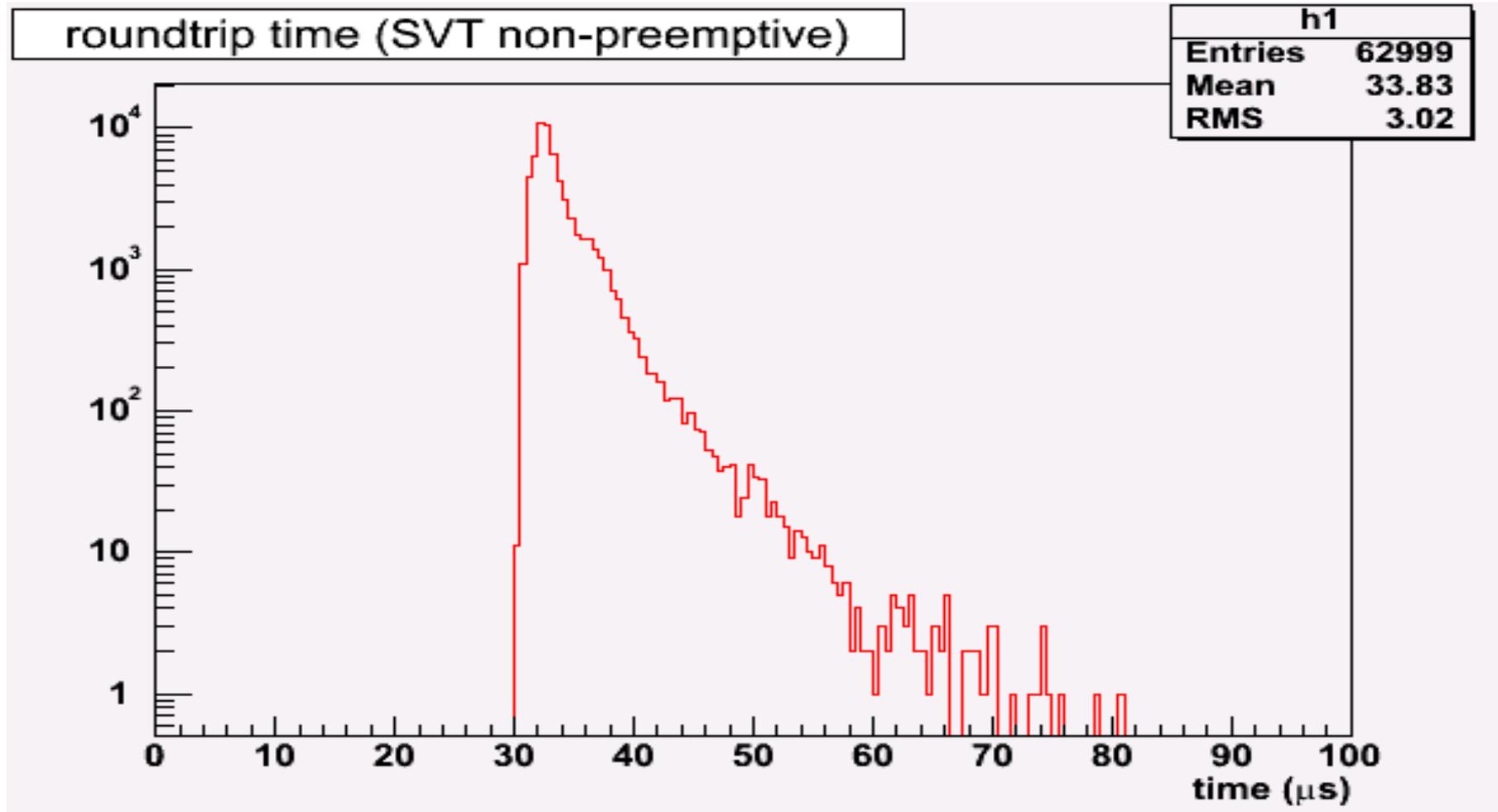
# “Mutli-homed” S-LINK

- CERN FILAR code changed to accommodate multiple s32PCI64's
- s32PCI64's run on separate PCI buses to prevent contention
  - a possible alternative: the “true” FILAR
    - would permit the use one less PCI bus
    - possibly save \$\$\$ ( PC & S-LINK )
    - requires HOLA?
    - not as mature as s32PCI64

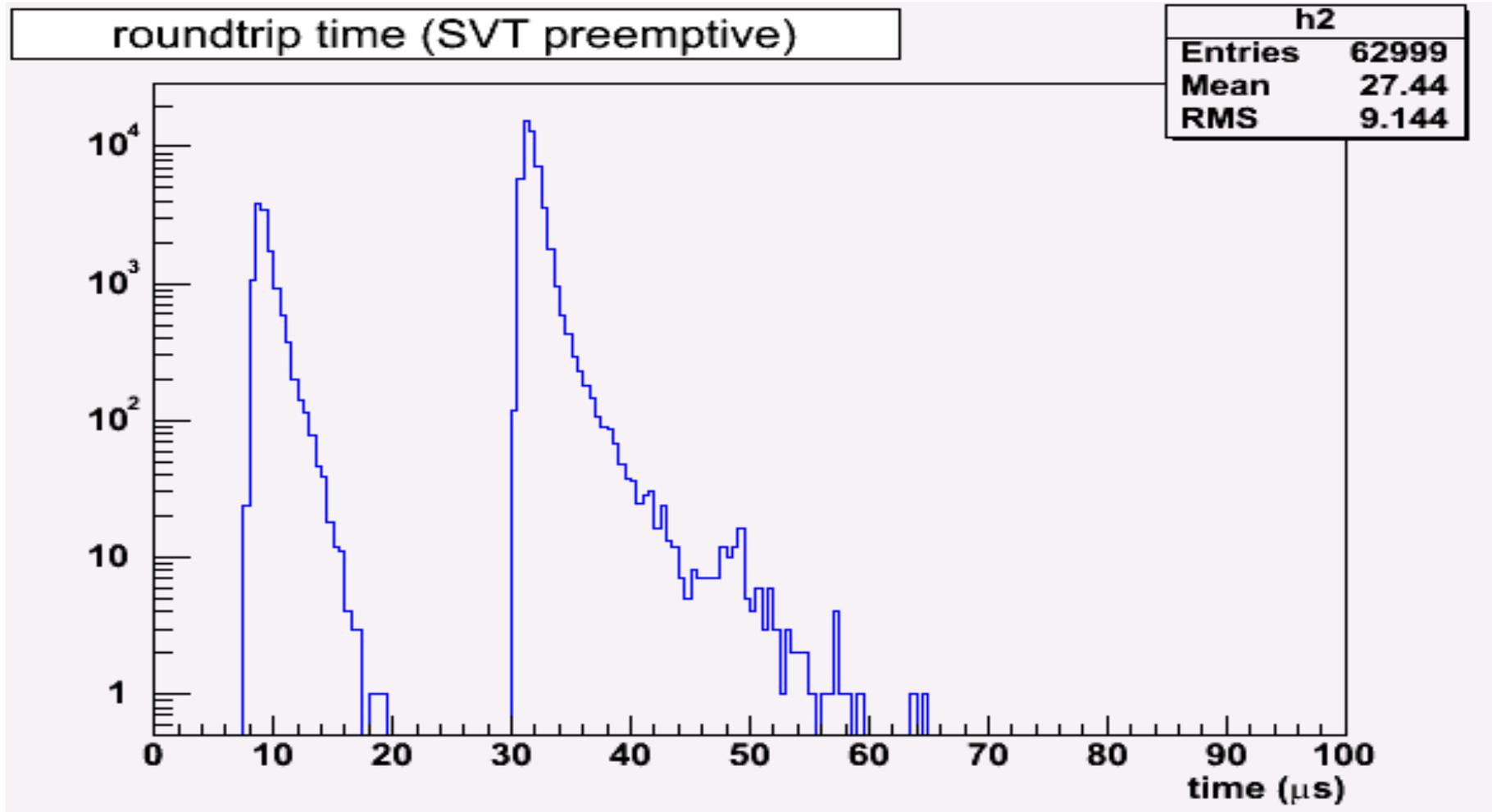
# Round trip Timing (setup)

- Fake L1A's in vxWorks instruct two PULSAR's to feed the PC, the PC returns decisions to one of them
- SVT delayed  $\sim 20\mu\text{s}$  from first L1A.
  - `usleep()` is a no-op in vxWorks
  - use `vxTime()`, time stamp and clock speed instead
    - see  $+10\mu\text{s}$  offset from the set delay
- $\Delta t$  measured from first L1A until the decision arrives using Tomi's F.W.
- Events are sent synchronously
  - doesn't model pile up from multiple buffers

# Round trip Timing (results 1)



# Round trip Timing (results 2)



# To-Do

- Use a distribution of SVT latencies
- Process non-SVT triggers for higher buffers while waiting for SVT data from lower buffers
  - relevant for Phase I : 4 buffers & 1 CPU
  - counter to keep track of skipped SVT info
  - prefer to wait for F.W. (vs. vxWorks) for asynchronous data transmission and reception
- Communicate trigger decisions to L2TS PULSAR