

L2 Node Architecture Tests

Kristian Hahn
University of Pennsylvania
08/16/04

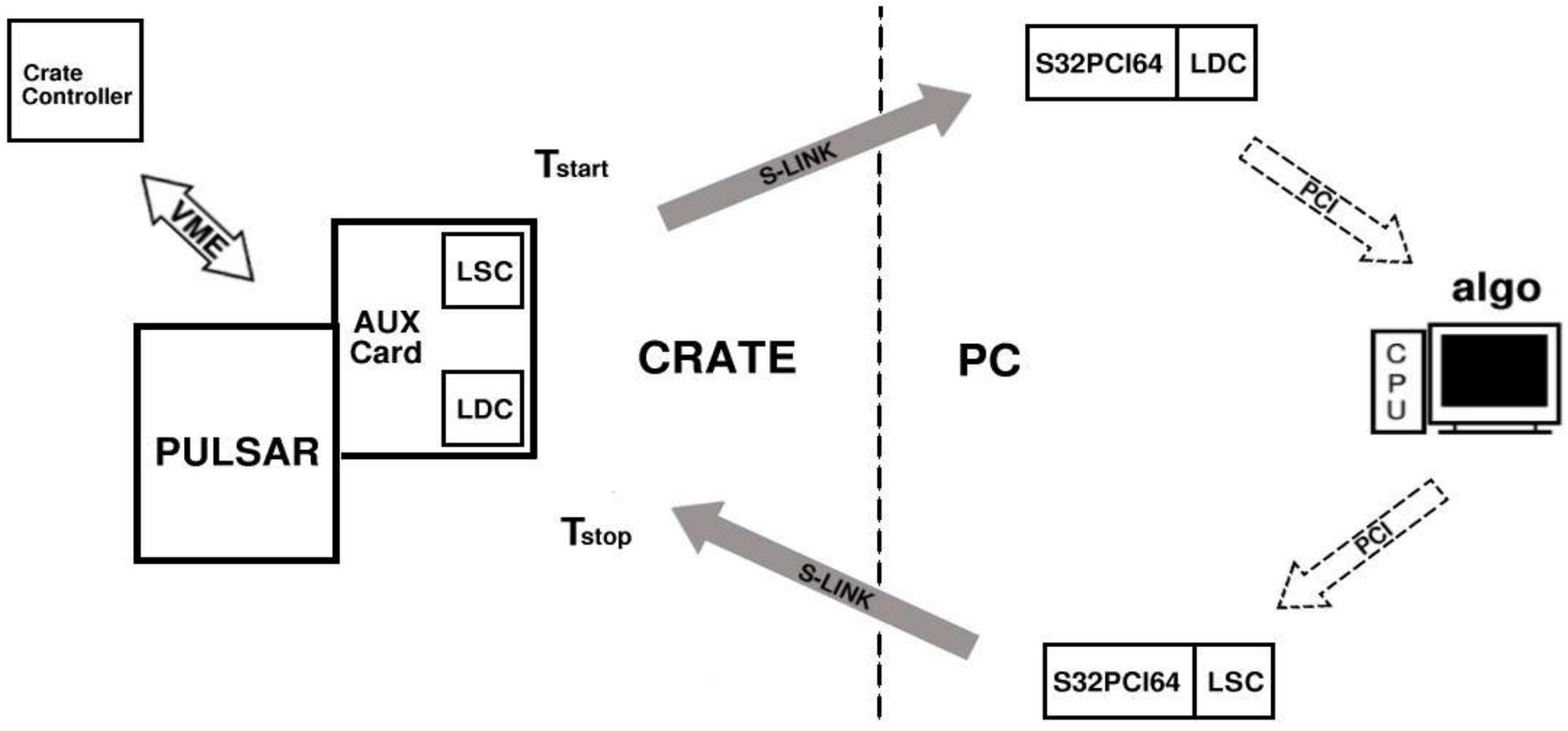
Big Picture

- Goal: Try to minimize the time for the L2 node to reach and relay a trigger decision. We want ...
 - Low latency (fast I/O)
 - Fast algorithm processing
- Test these aspects using ...
 - Modern dual processor machines
 - PULSAR/S-Link to source and sink data
 - Real physics data (from TL2D)
- This allows us to ...
 - Compare performance of different computing architectures
 - Optimize code for those architectures

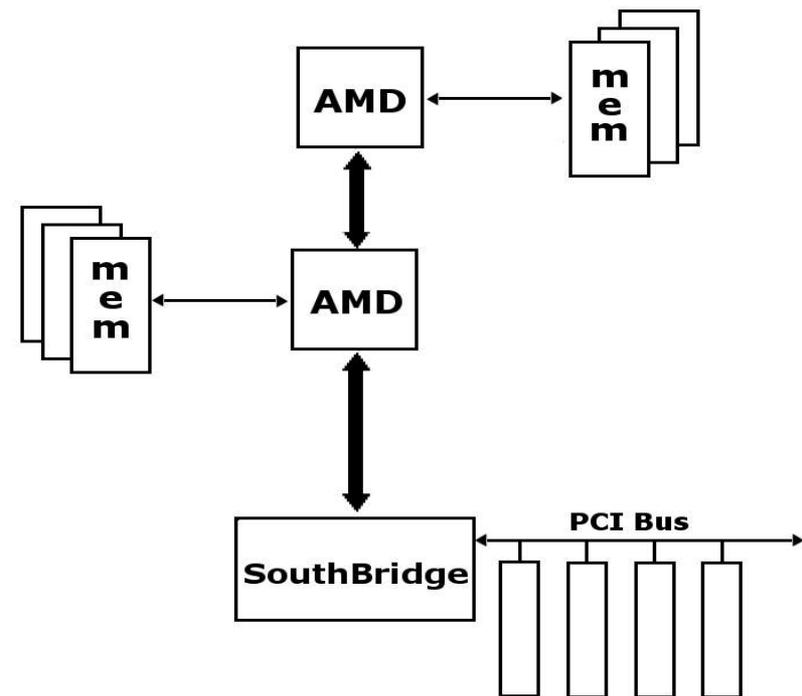
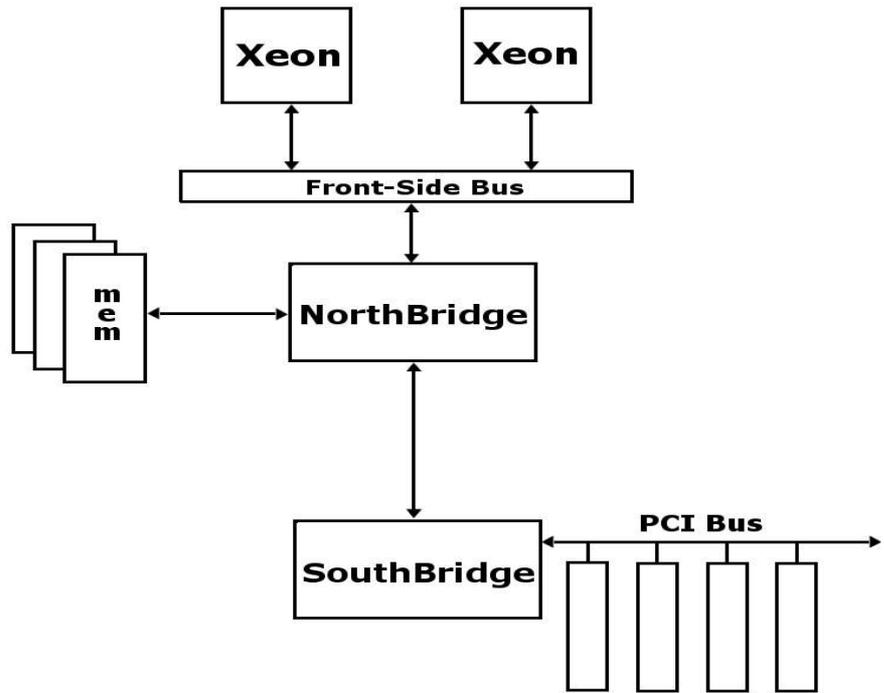
Architecture Tests

- Measurements
 - Algorithm Time
 - Indicates raw computing performance
 - PHYSICS-1_04-v6
 - Roundtrip Time (w/o algos.)
 - I/O latency, minimal computation
 - Roundtrip Time (w/ algos.)
 - Similar to expected operational environment
- Platforms
 - 2x Xeon 2.4 GHz, 3.2 GHz
 - 2x Opteron 2.4 GHz
 - Alpha 500 MHz

Test Setup (roundtrip)

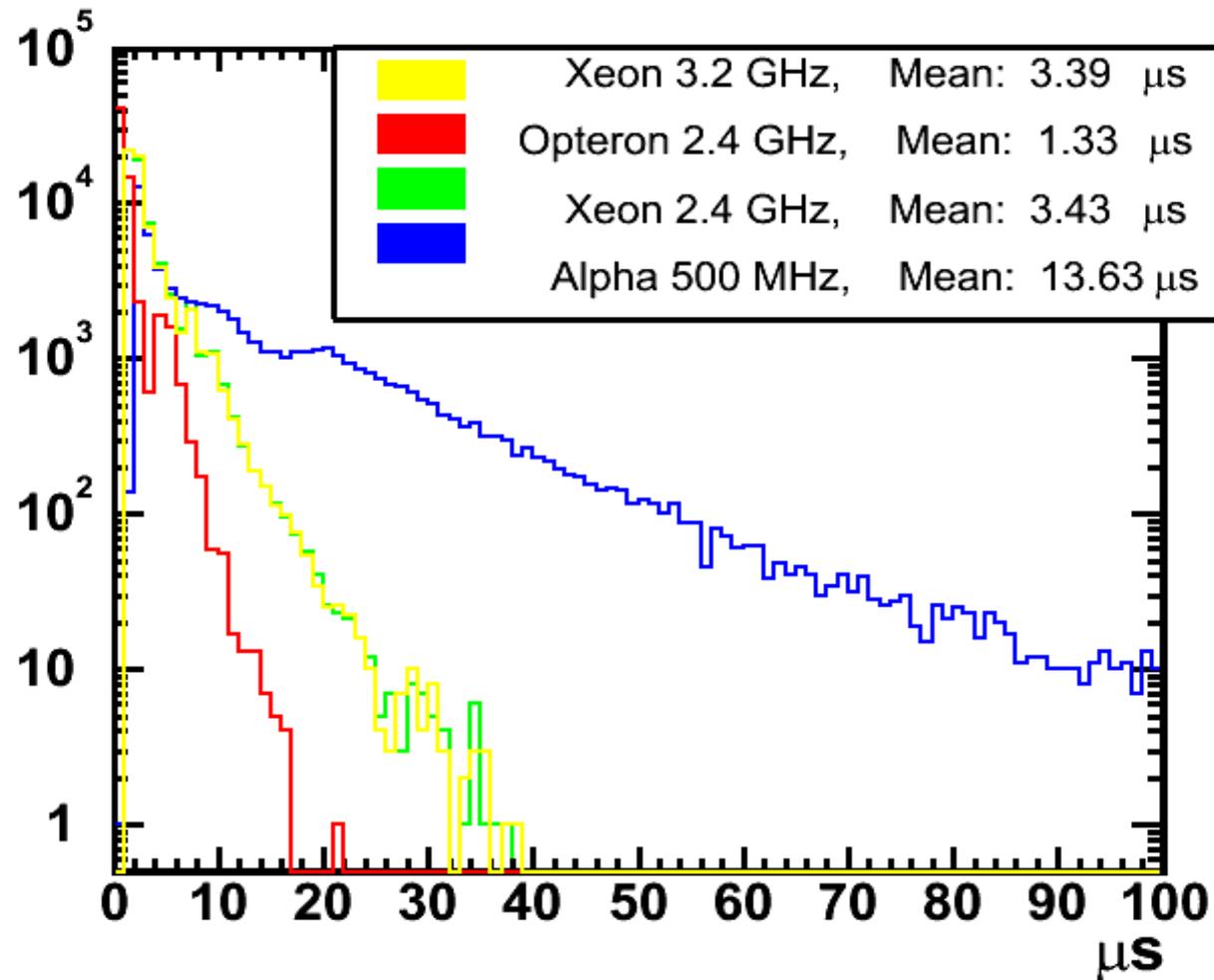


Architecture Review : Xeon vs. Opteron

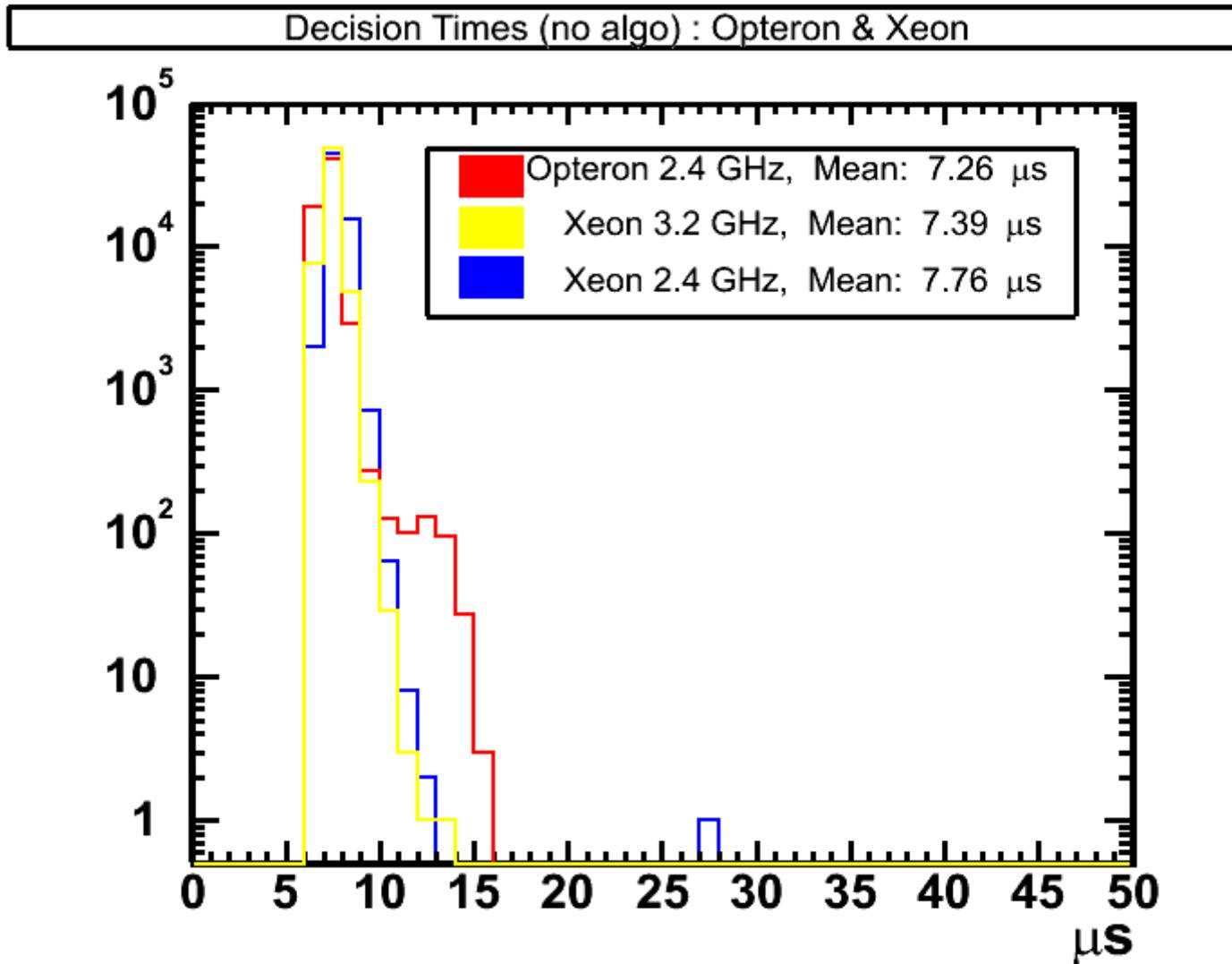


Algorithm Time

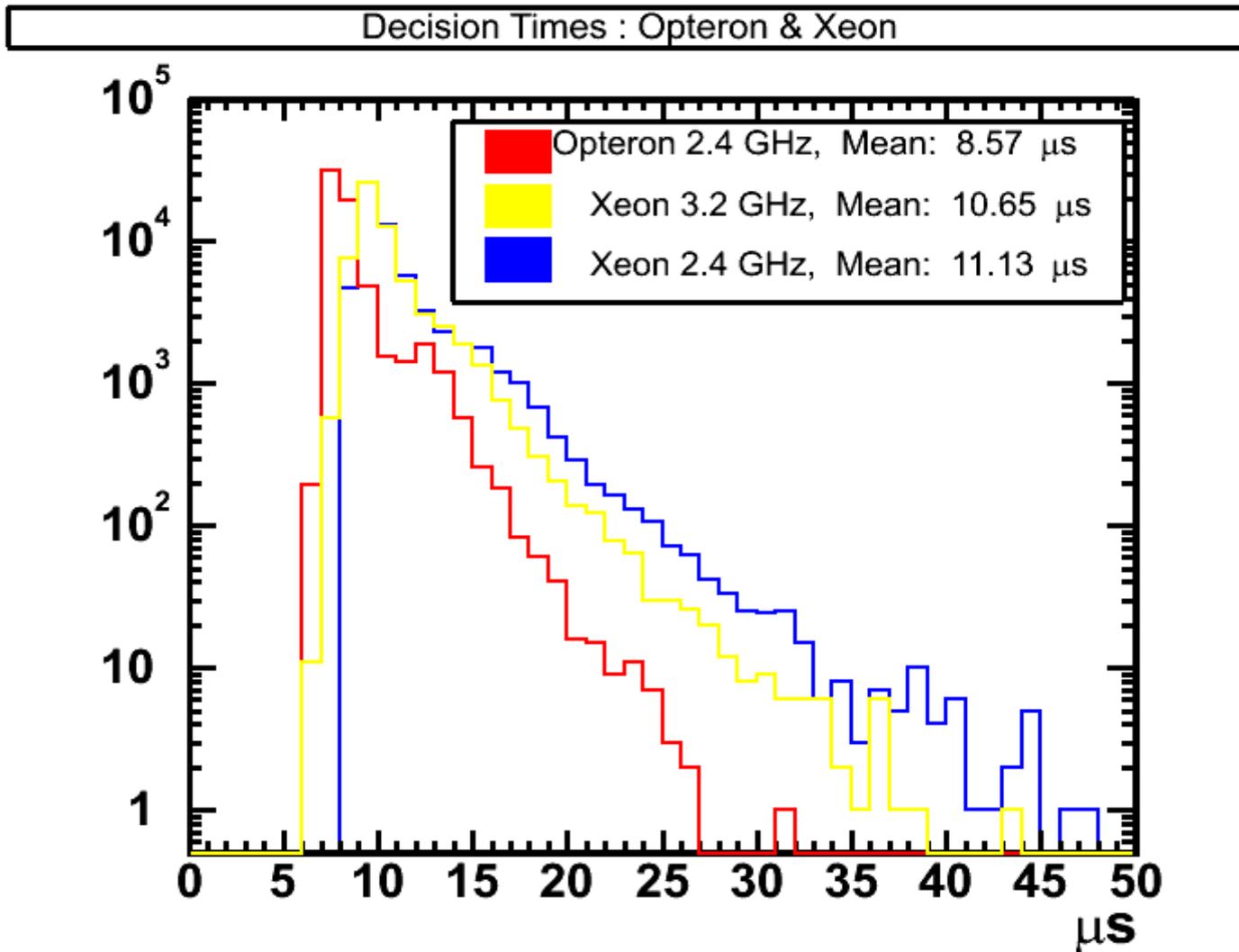
Algorithm Times : Opteron, Xeon & Alpha



RoundTrip Time (w/o algos.)



RoundTrip Time (w/ algos)



Conclusions

- Results are VERY preliminary ...
 - Repeat AMD & Xeon 3.2 measurements
 - Xeon 3.2 results are surprising
 - AMD looks good, have to be sure
- Definitely I/O bound